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Compal Confidential

HTW20 LA-3171P Schematics Document

Intel Yonah/Merom with 945PM/GM + DDRII + ICH7M
(+VGA/B ATI M52P/M54P/56P)

2006-04-26

REV: 1.0

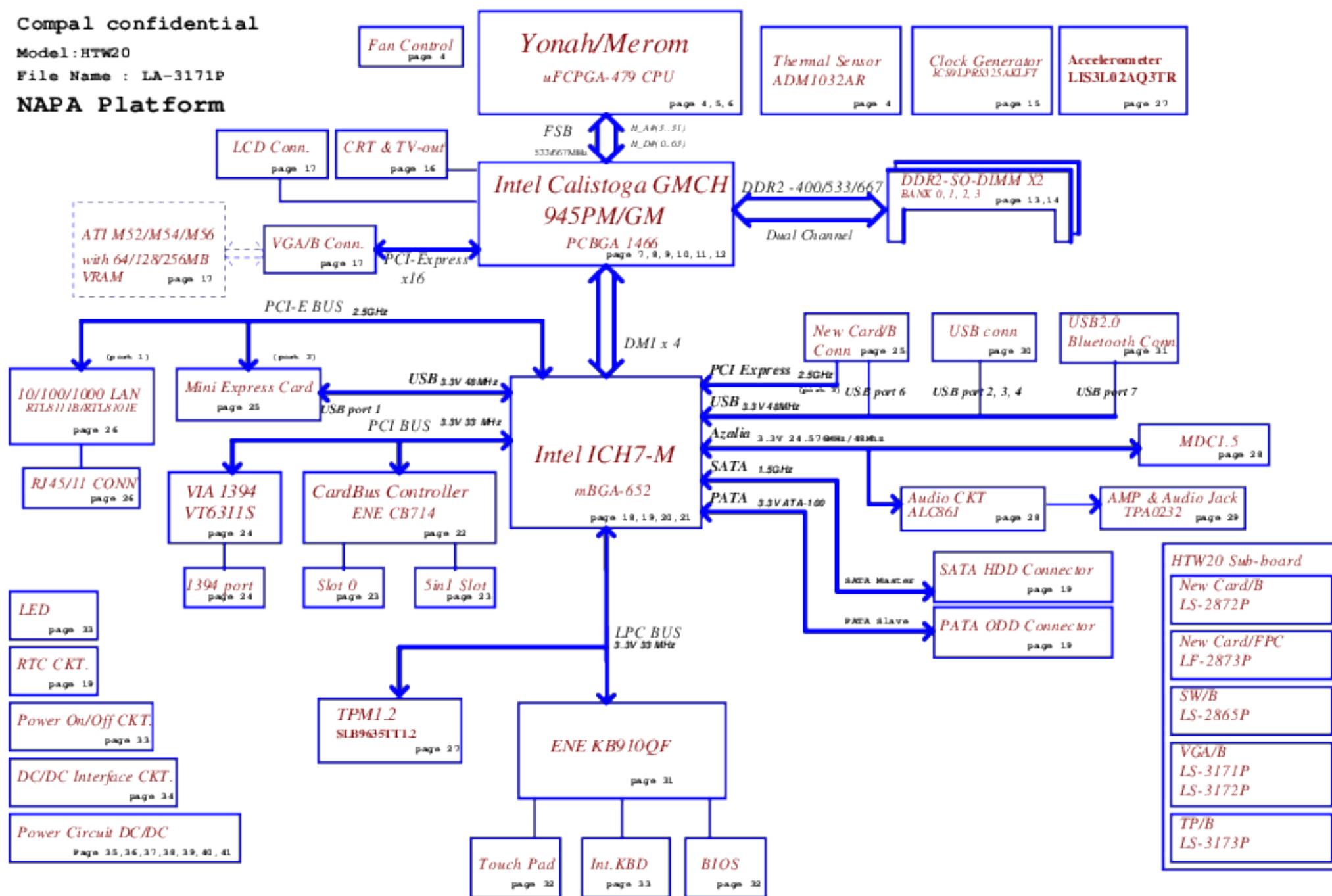
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04/26/2006	04/26/2006	HTW20 M/B LA-3171P	1.0	1.0

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Model: HTW20

File Name : LA-3171P

NAPA Platform



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Block Diagram

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Voltage Rails

Power Plane	Description	S1	S2	S3
VIN	Adapter power supply (12V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	CORE voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR termination	ON	OFF	OFF
+1.0V	1.0V switched power rail	ON	OFF	OFF
+1.1V	1.1V switched power rail	ON	ON	OFF
+1.2V	1.2V switched power rail	ON	OFF	OFF
+2.5V	2.5V switched power rail	ON	OFF	OFF
+3.3V	3.3V always on power rail	ON	ON	ON*
+3.3V	3.3V switched power rail	ON	OFF	OFF
+5V	5V always on power rail	ON	ON	ON*
+5V	5V switched power rail	ON	OFF	OFF
+5VSB	+5VSB always on power rail	ON	ON	ON*
+RTCNOO	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	IRQ / GNT #	PIRQ
1584	B0	A#1:0	0	E
CA BD IICB	B4	A#2:0	2	A, B
SMSI	B4	A#2:0	2	A, B

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SMSI 24C16	A#0	1 0 1 0 0 0 0 Xb
SMSI SMA 8T 8A TINY	1#0	0 0 0 1 0 1 1 Xb
SMSI ADM 0192	9#0	1 0 0 1 1 0 0 Xb
CPU THERM ALGO NTR		

ICH7-M SM Bus address

DEVICE	HEX	ADDRESS
DDR RD - DMM 0	A#0	1 0 1 0 0 0 0 0
DDR RD - DMM 1	A#4	1 0 1 0 0 1 0 0
CLOCK GEN IN RA TO R (EXT)	B#2	1 1 0 1 0 0 1 0

Board ID / SKUID Table for AD channel

Vdd	3.3V +/- 5%			
Rin	100K +/- 5%			
Board ID	Rin	VAD_RIN_min	VAD_RIN_TYP	VAD_RIN_max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	35K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	01
1	02
2	03
3	
4	
5	
6	
7	

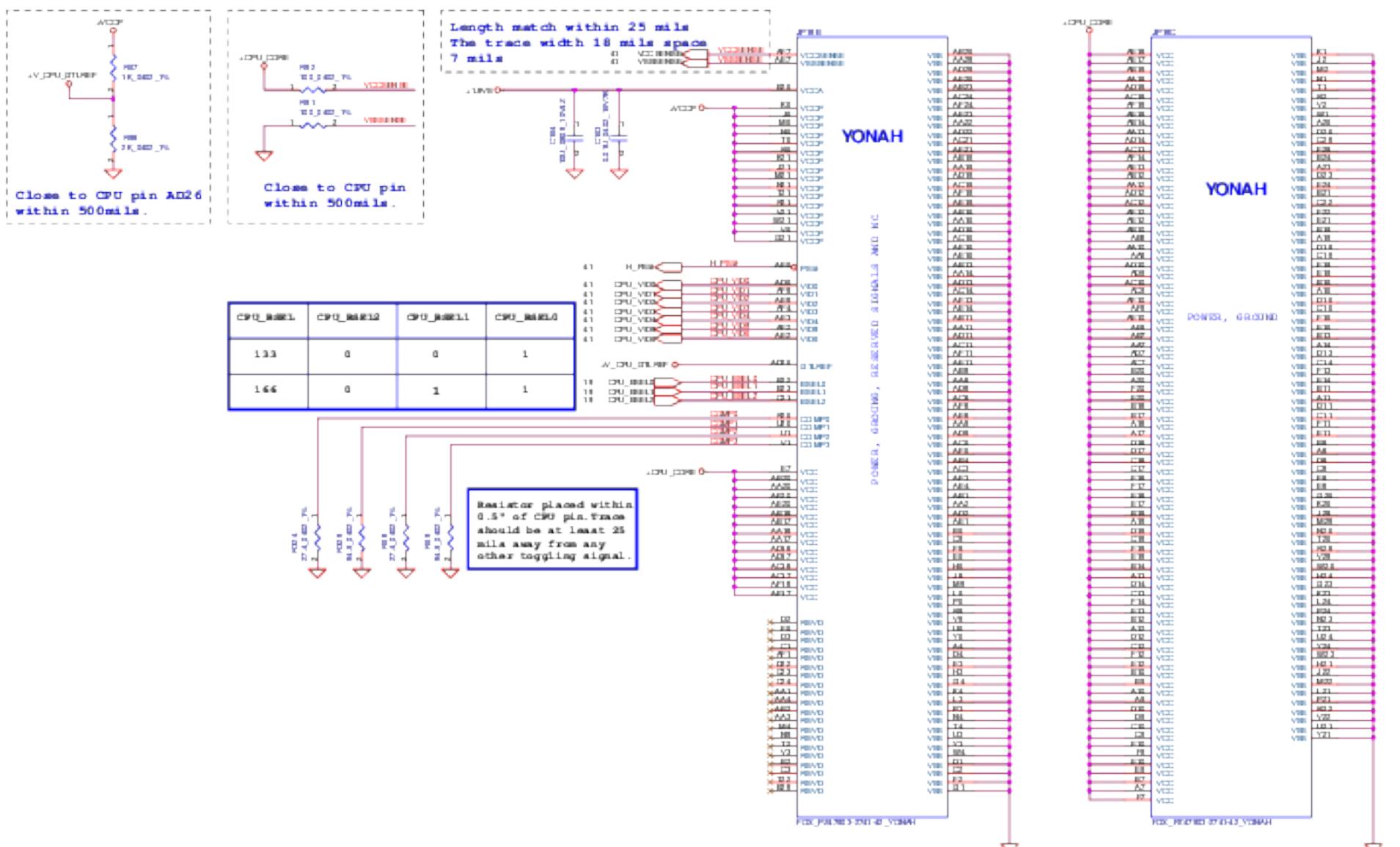
BTO Option Table

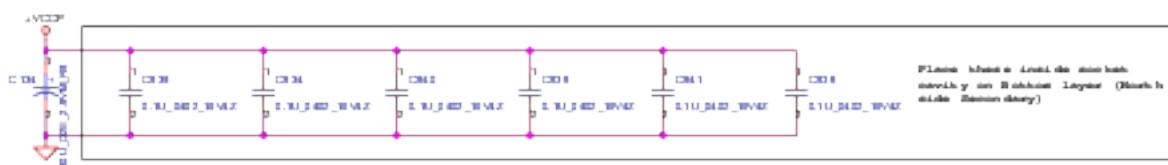
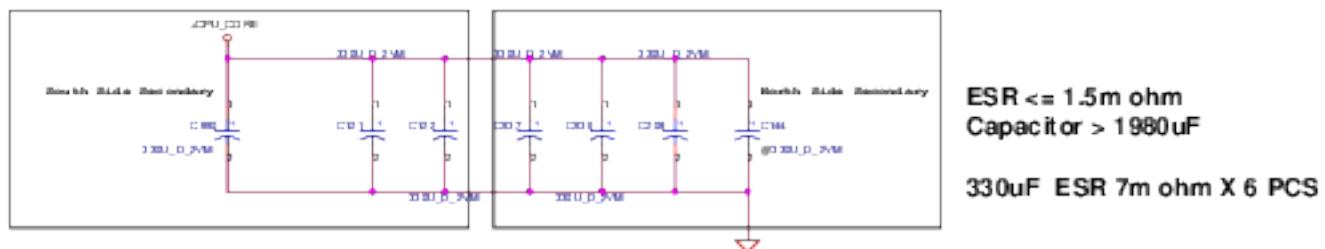
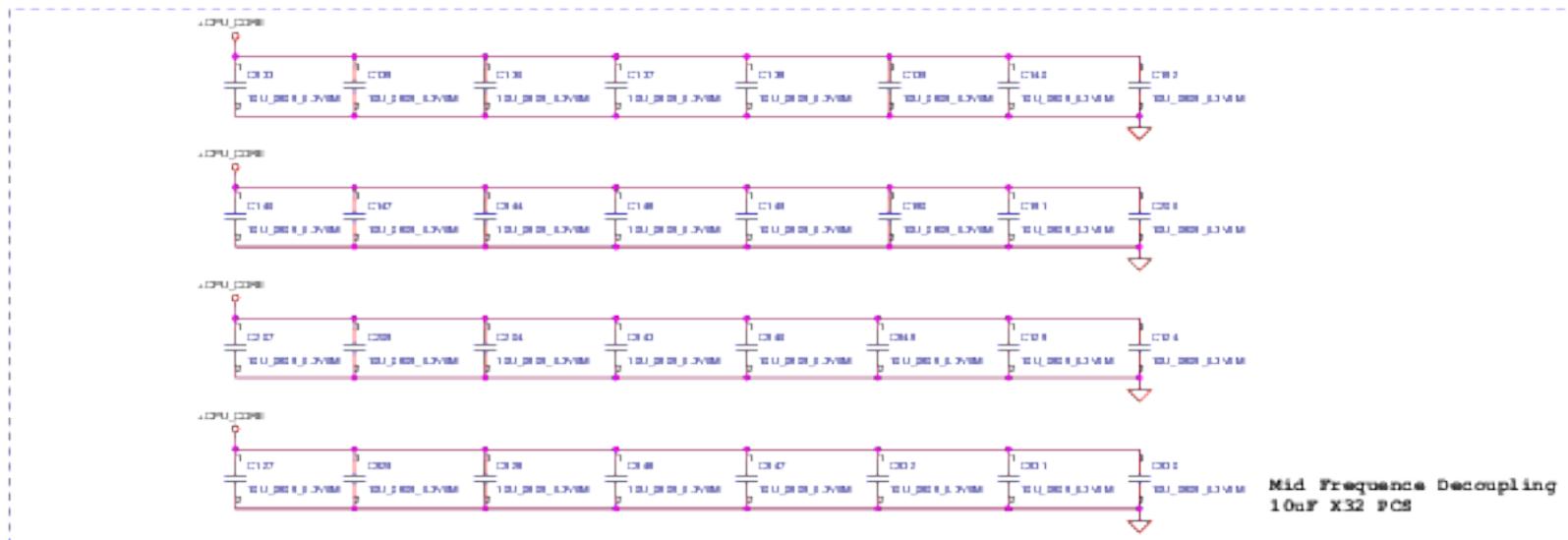
BTO Item	BOM Structure
VGA	PN#
New Card	NEWCARD#
Giga LAN	100M#
KILL SW	WLAN#
BlueTooth	BT#
SIM1	SIM1#

SKU ID Table

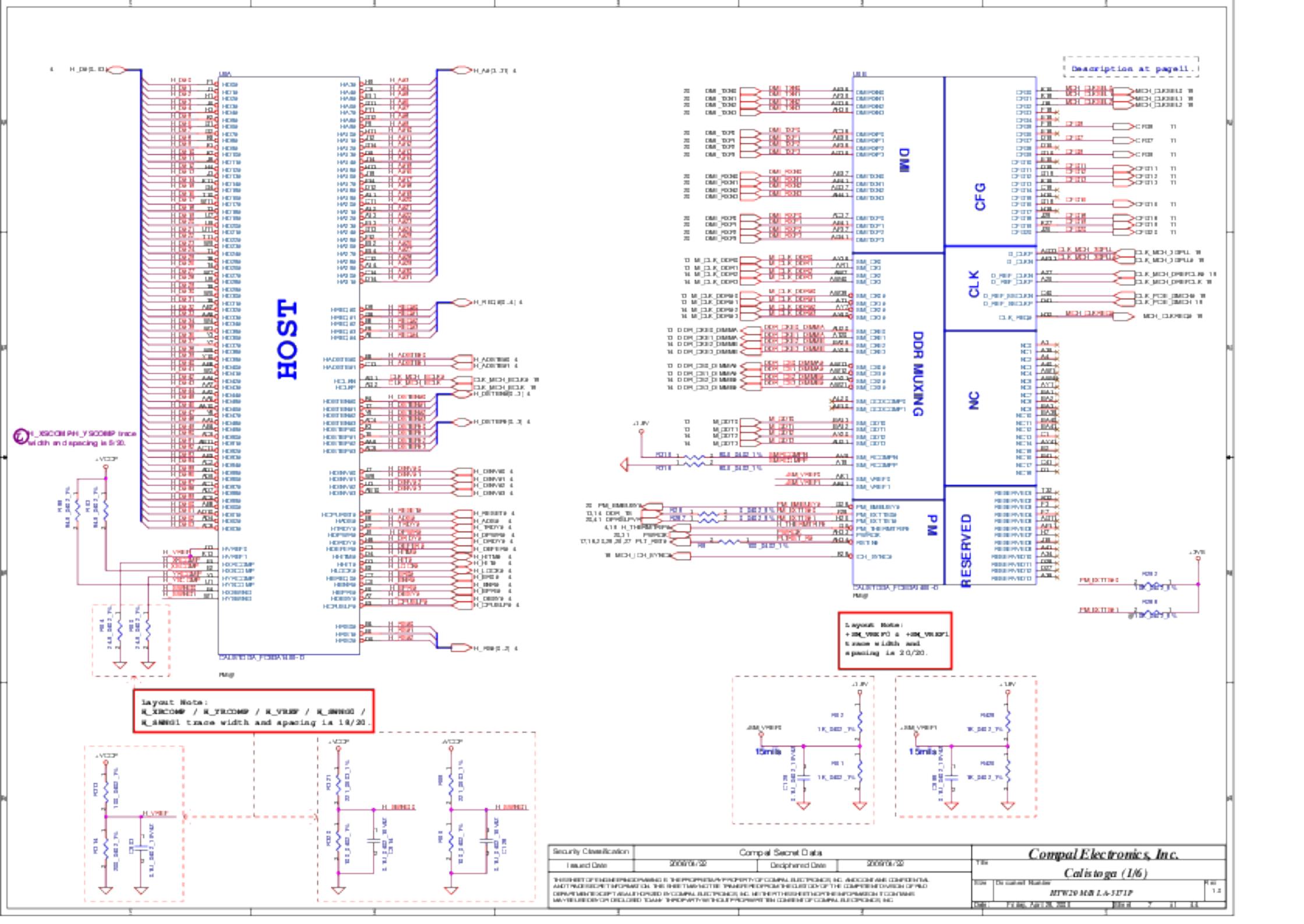
SKU ID	SKU
0	
1	
2	
3	
4	
5	
6	
7	

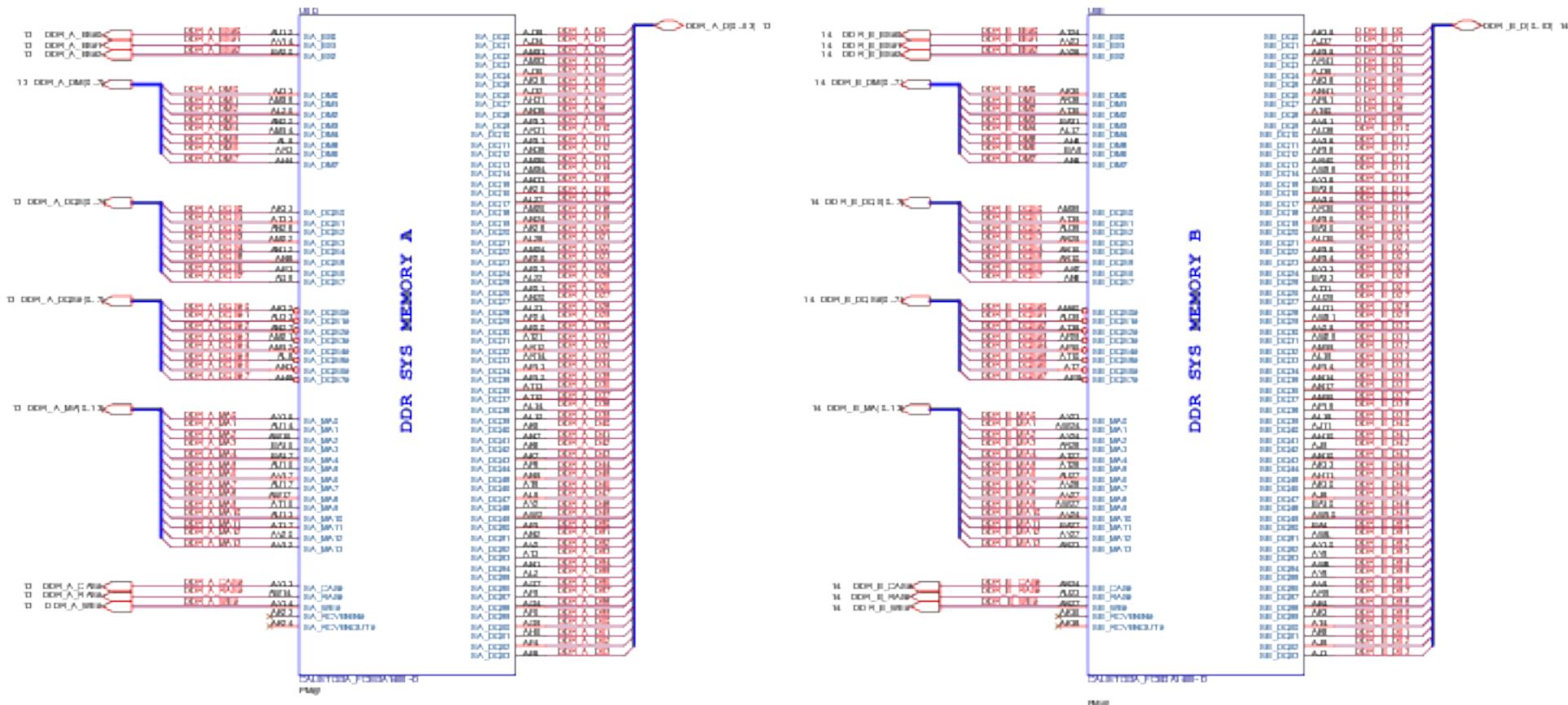
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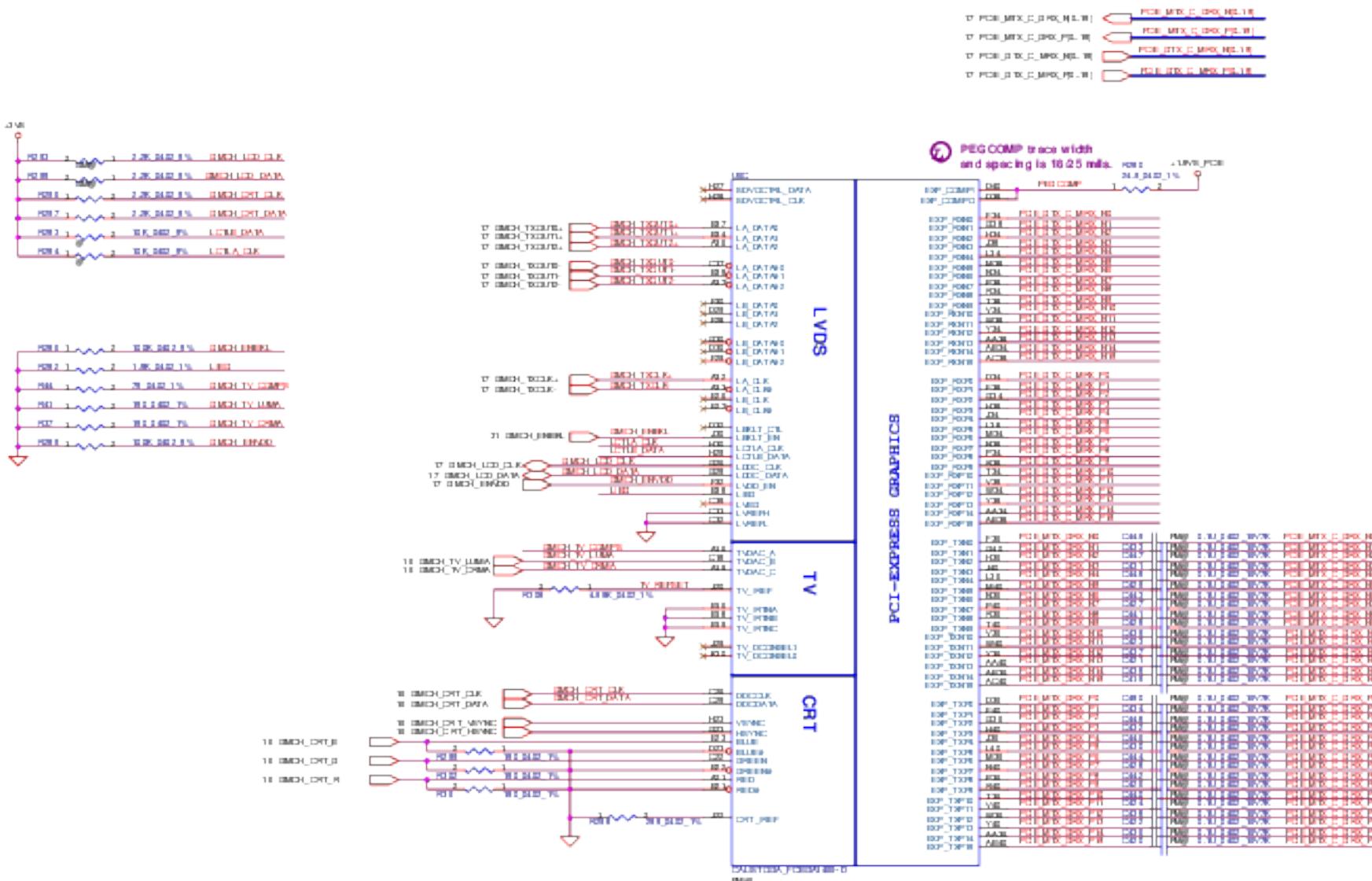


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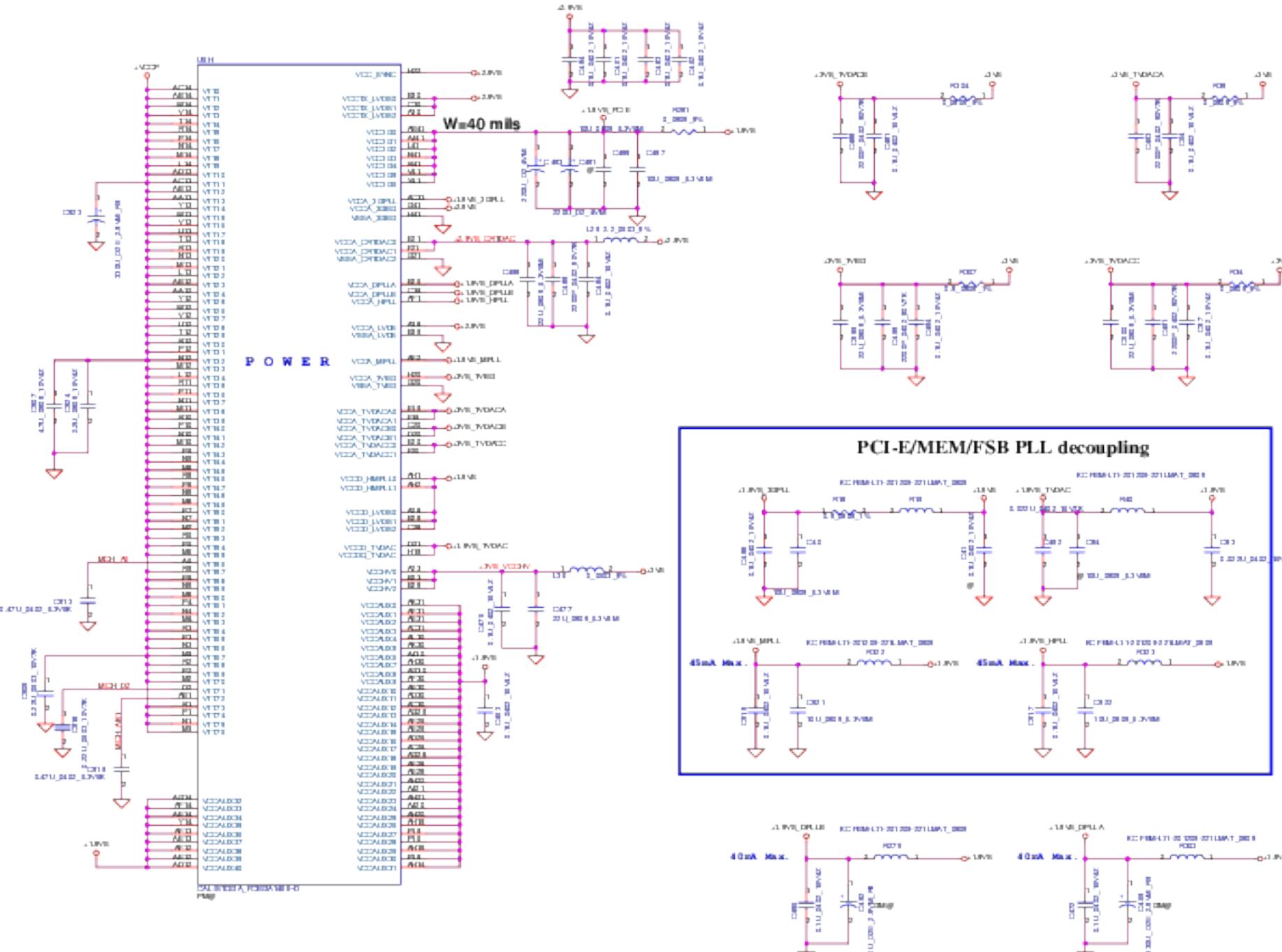




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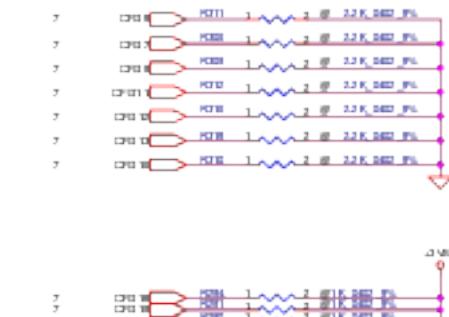
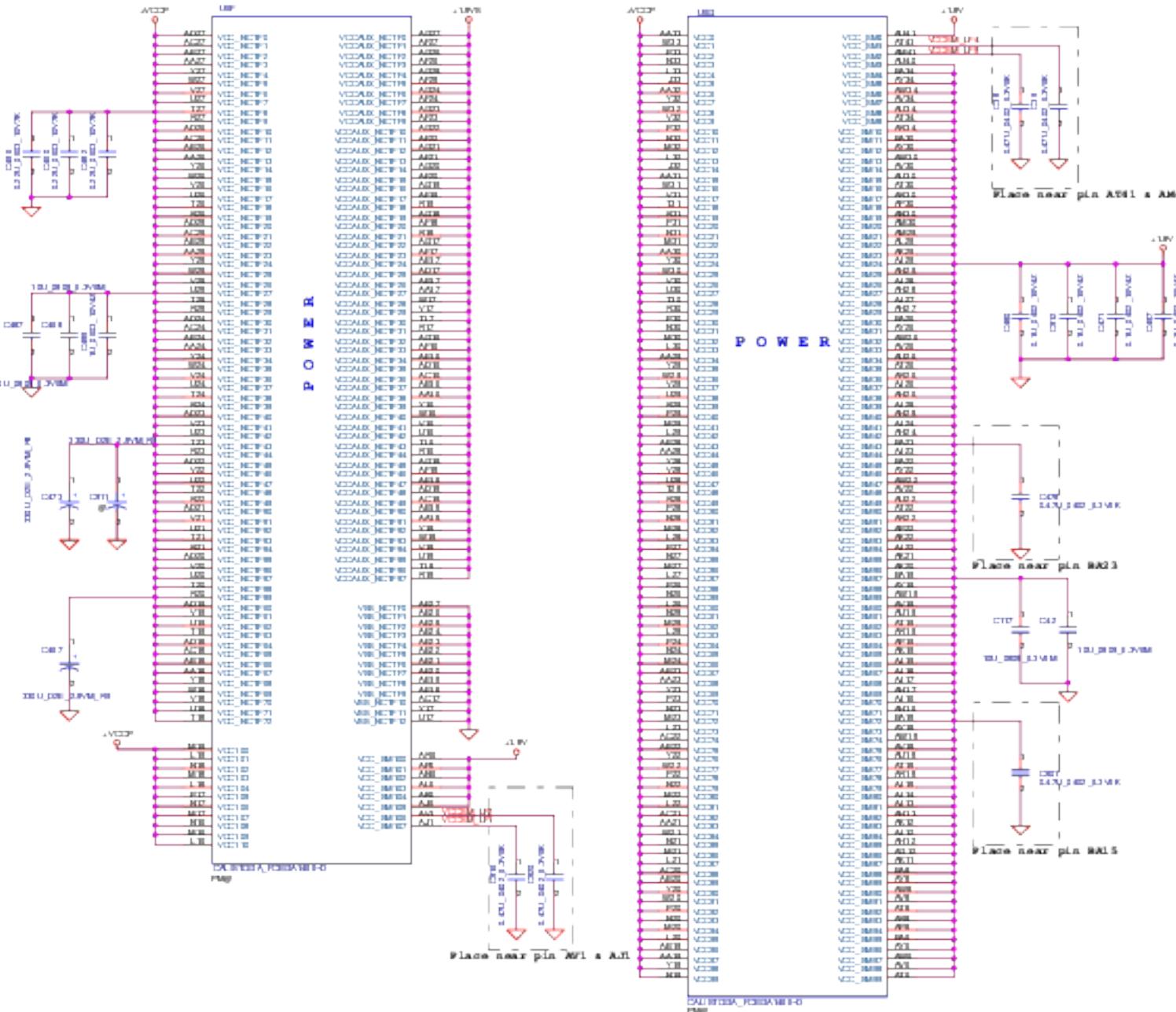
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Strap Pin Table

crs[3:17] have internal pull up
crs[18:19] have internal pull down

CRS [2:0]	011 = 440MHz/a RAM 001 = 533MHz/a RAM
CRS5	0 = DME x 2 1 = DME x 4 *(default)
CRS0	0 = Reserved 1 = Mobile Yonah CRU*(Default)
CRS9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CRS11	0 = Reserved 1 = Calistoga *
CRS[13:12]	00 = Reserved 01 = XDR Mode Enabled 10 = All 2 Mode Enabled 11 = Normal Operation *(Default)
CRS16	0 = Dynamic CCR Disabled 1 = Dynamic CCR Enabled *(Default)
CRS18	0 = 1.8V *(Default) 1 = 1.5V
CRS19	0 = Normal Operation * (Default) 1 = DME Lane Reversal Enable
ADVO_CMRDATA	0 = No ADVO Device Present * (Default) 1 = ADVO Device Present
CRS20 (PCIE/ADVO select)	0 = only PCIE or ADVO is operational. *(default) 1 = PCIE/ADVO are operating simultaneously



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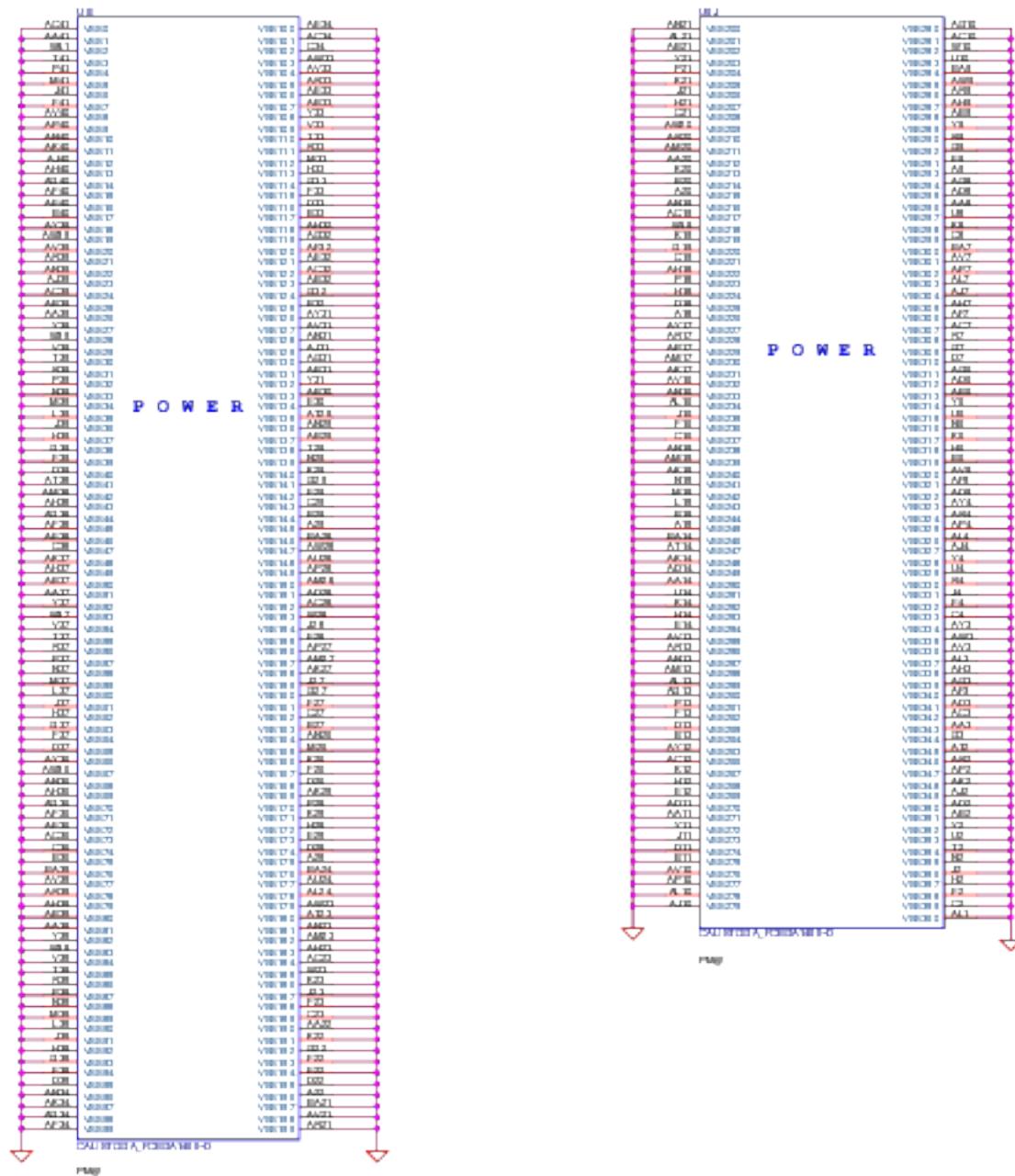
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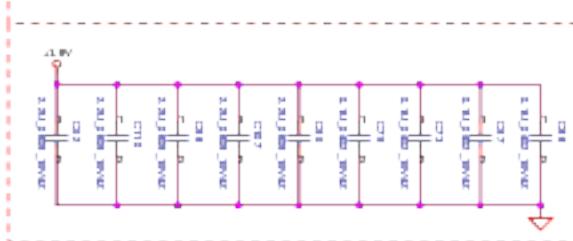
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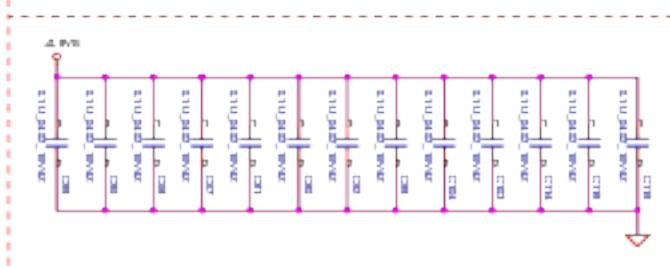
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II DDR_A_DQDATA_2
 II DDR_A_DQ_10
 II DDR_A_DM_2
 II DDR_A_DQDATA_7
 II DDR_A_DM_10

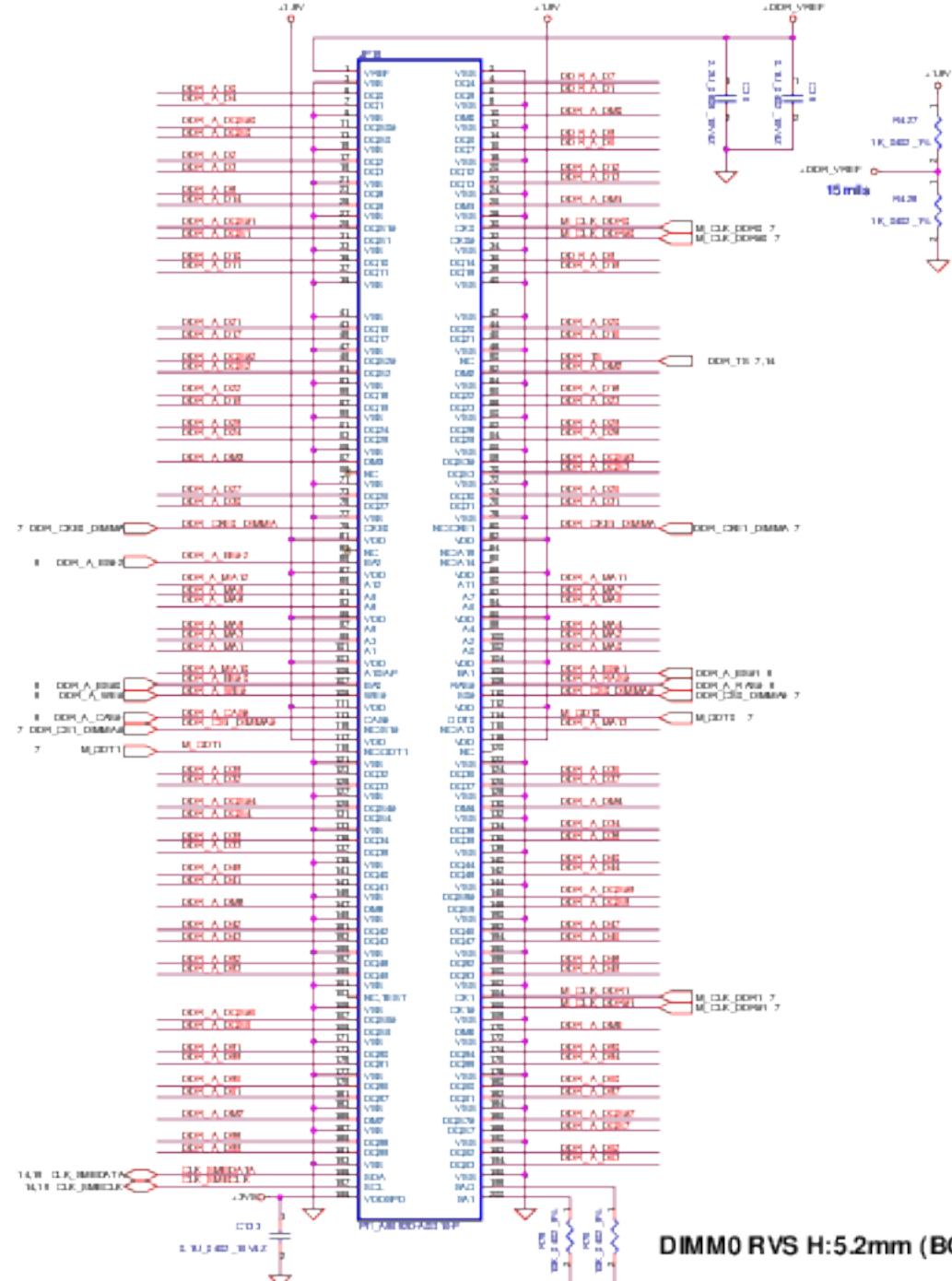
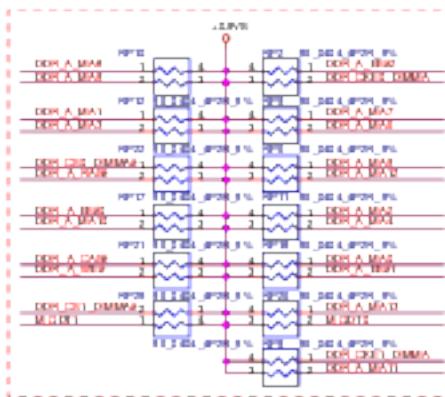
Layout Note:
Place near J P27



Layout Note:
Place a capacitor close to every 2 pullup resistors terminated to +0.9VBS



Layout Note:
Place these resistor closely JP27; all
trace length Max=1.5"



DIMM0 RVS H:5.2mm (BOT)

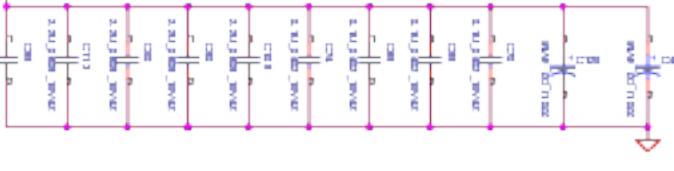
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DDR4-SODIMM SLOT I

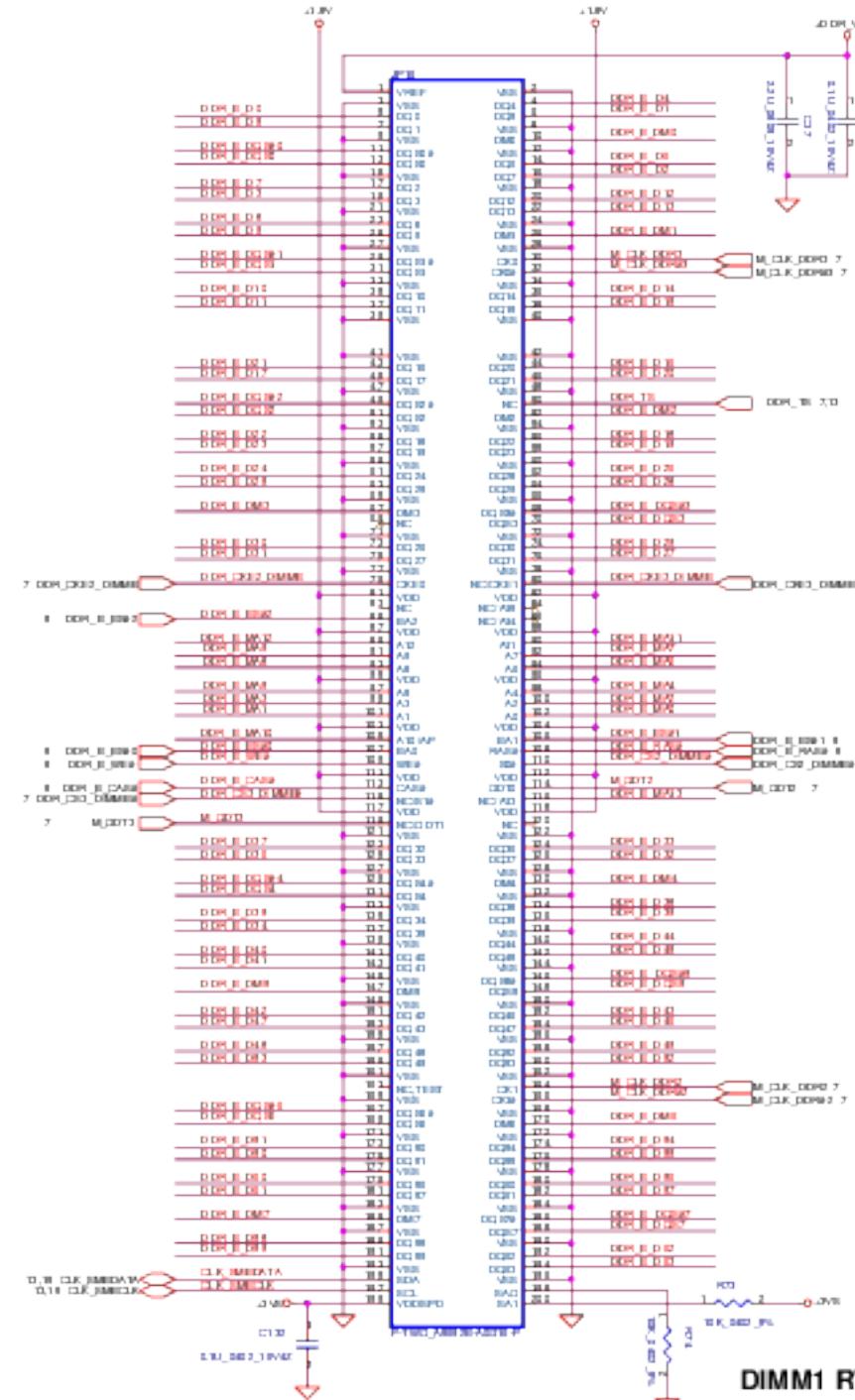
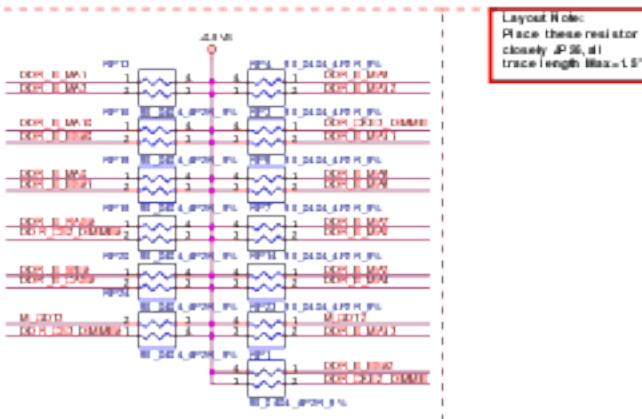
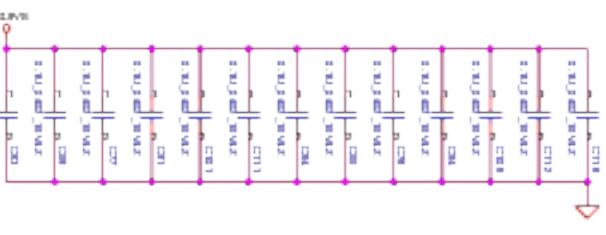
MTW20 MIN L4-JEDEC



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_S

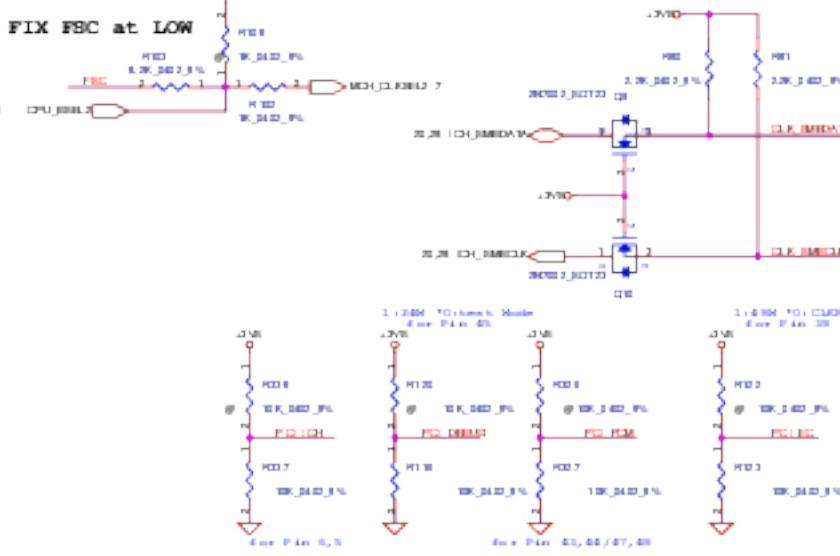
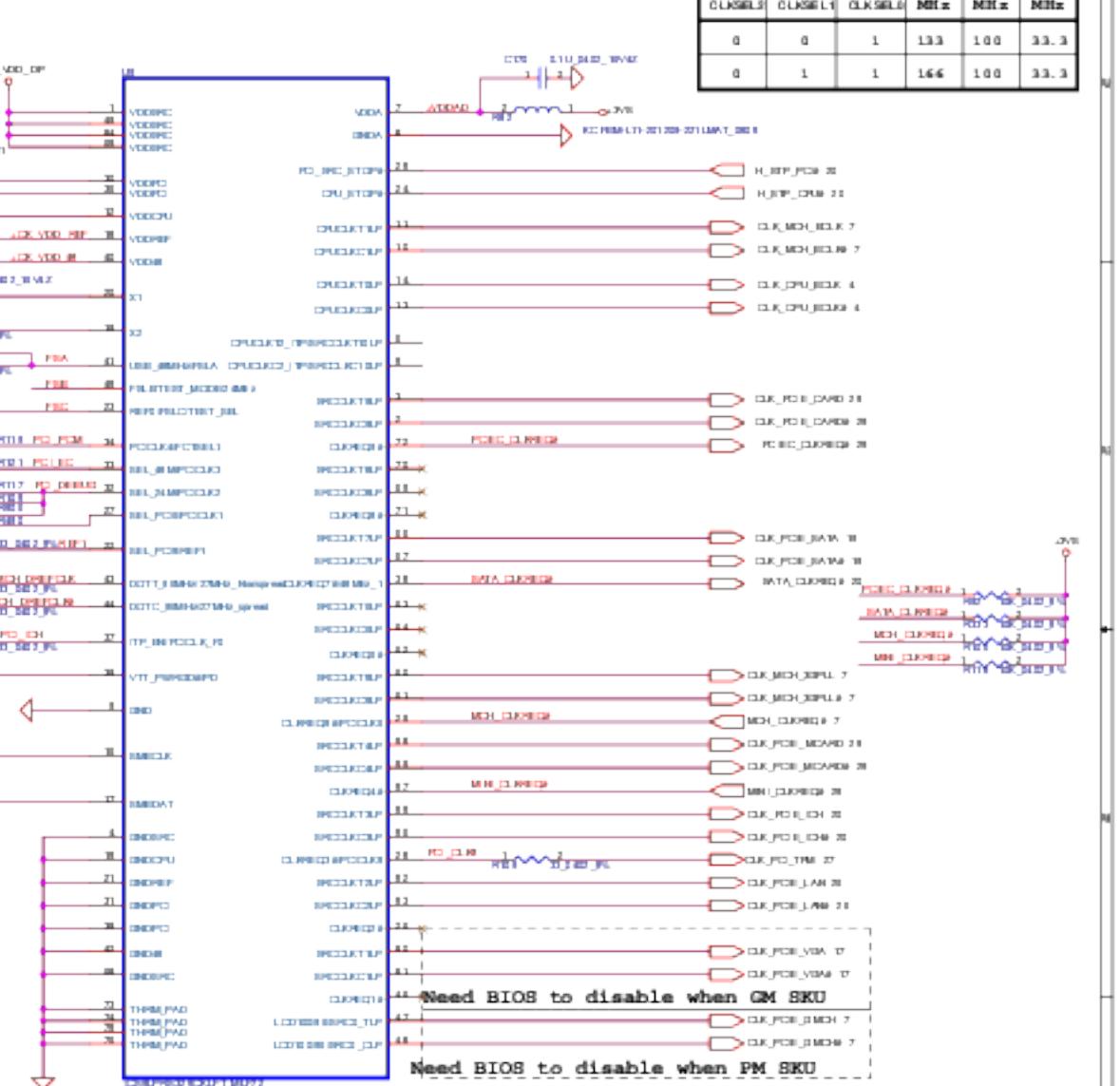
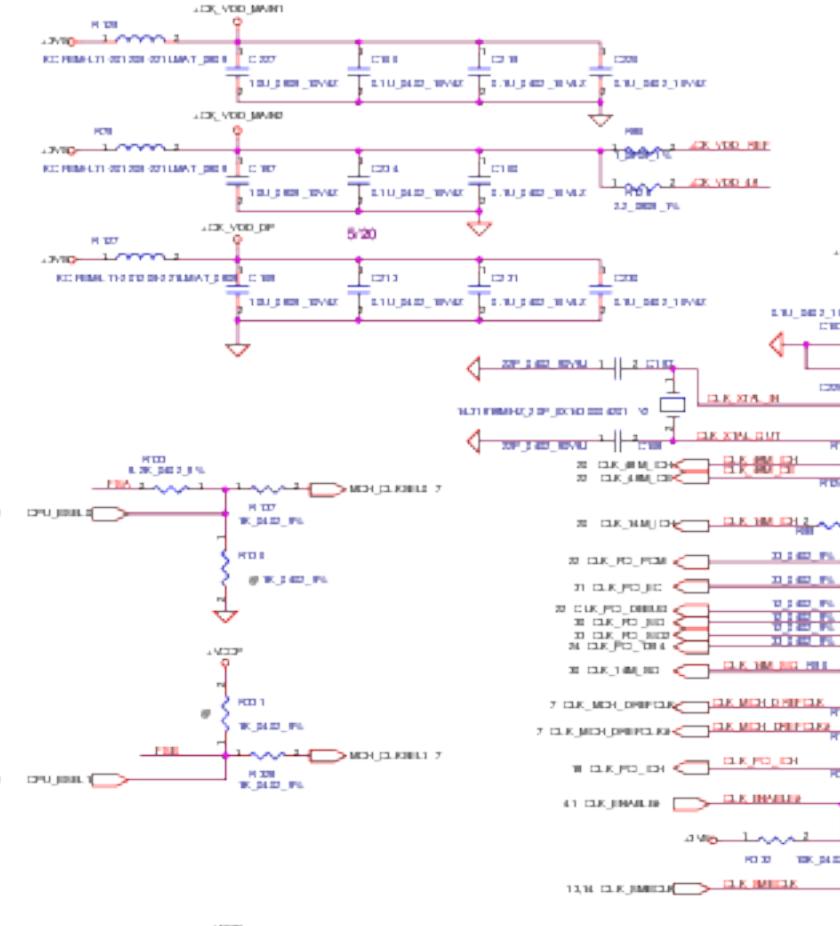


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_S



DIMM1 RVS H:9.2mm (BOT)

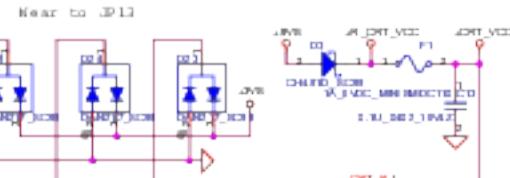
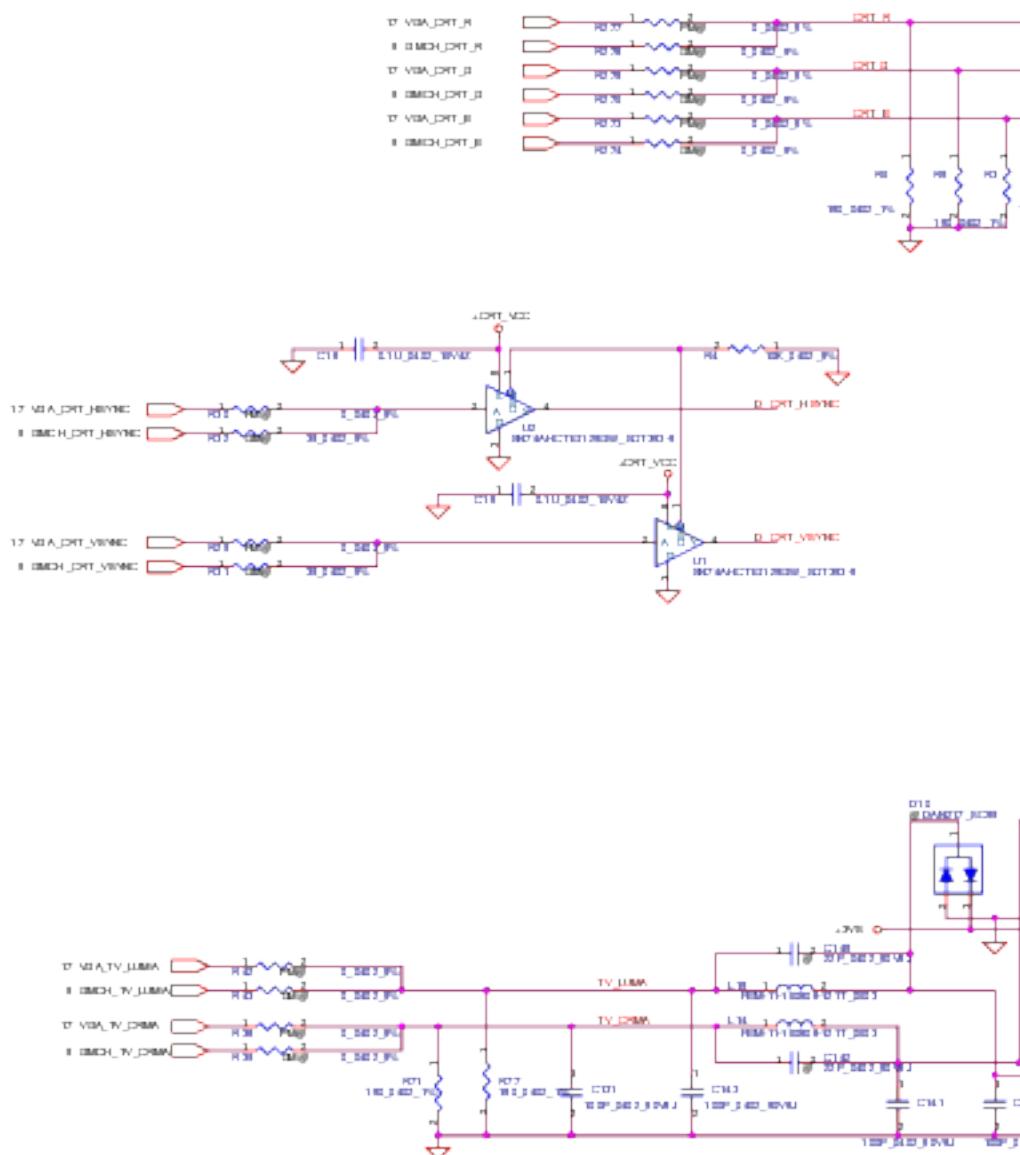
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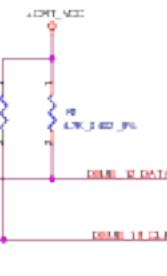
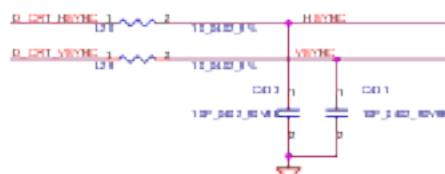
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CRT CONNECTOR

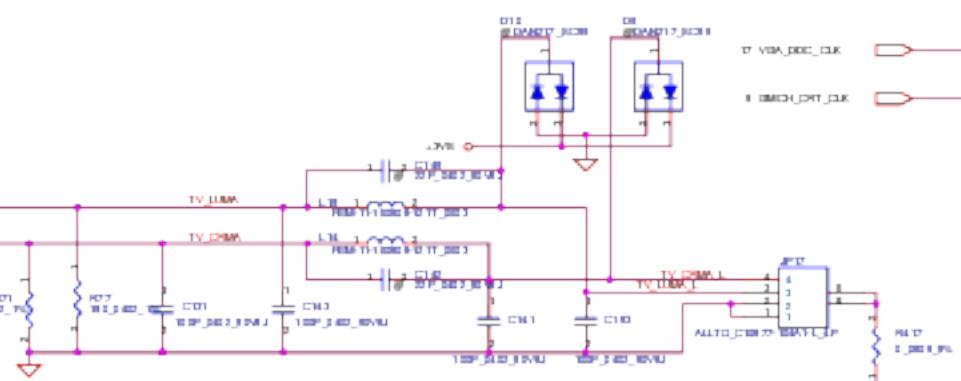
CRT Connector



CRT Conn.



TV-OUT Conn.



- 1. X ground
- 2. GND ground
- 3. Y (R/G/Cathode阴极)
- 4. C (G/Anode阳极)

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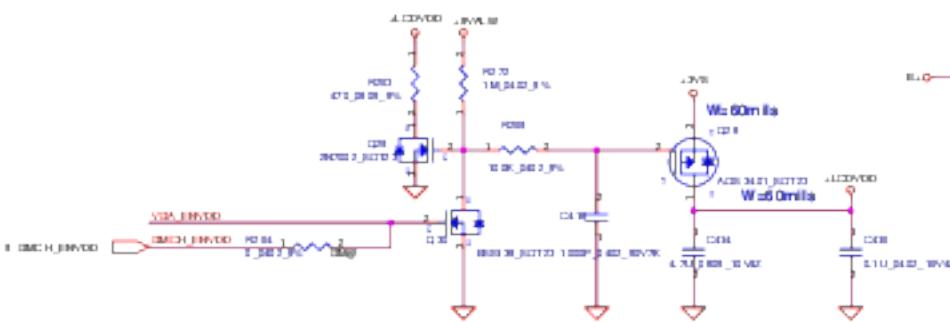
CRT & TVout Connector

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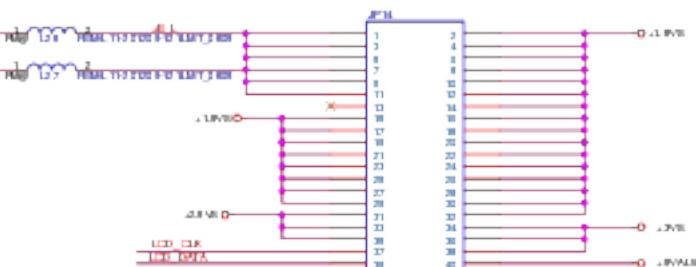
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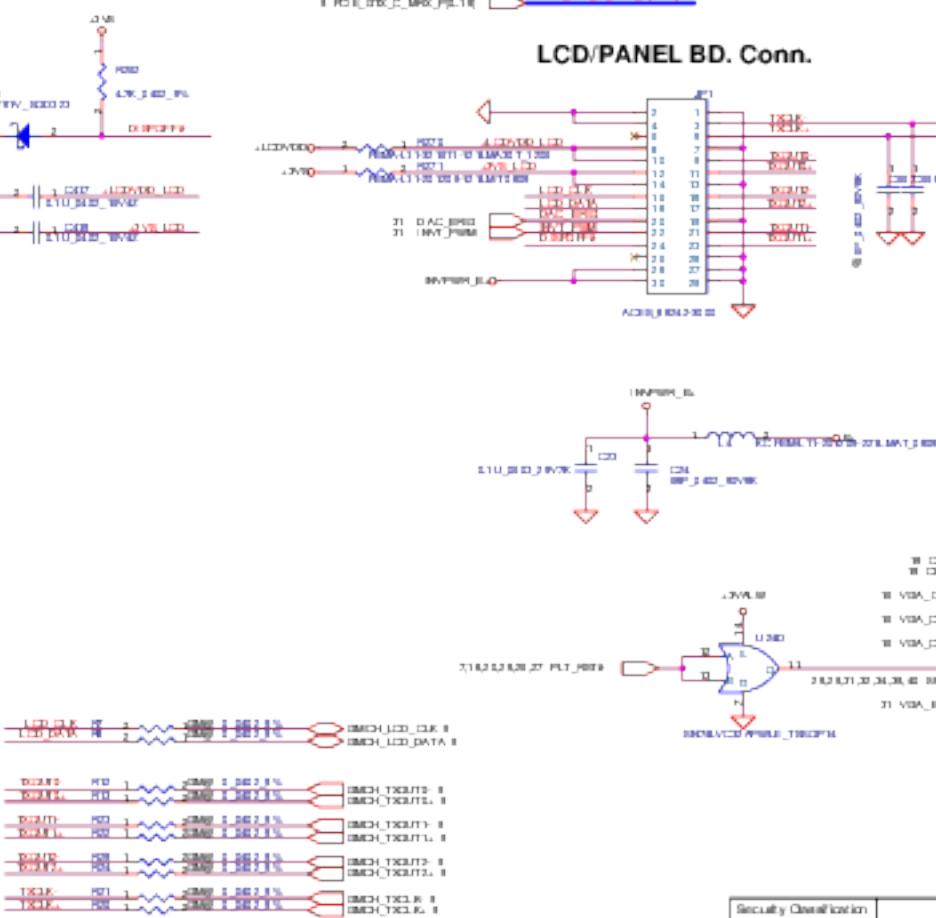
LCD POWER CIRCUIT



VGA BOARD Conn.



LCD/PANEL BD. Conn.



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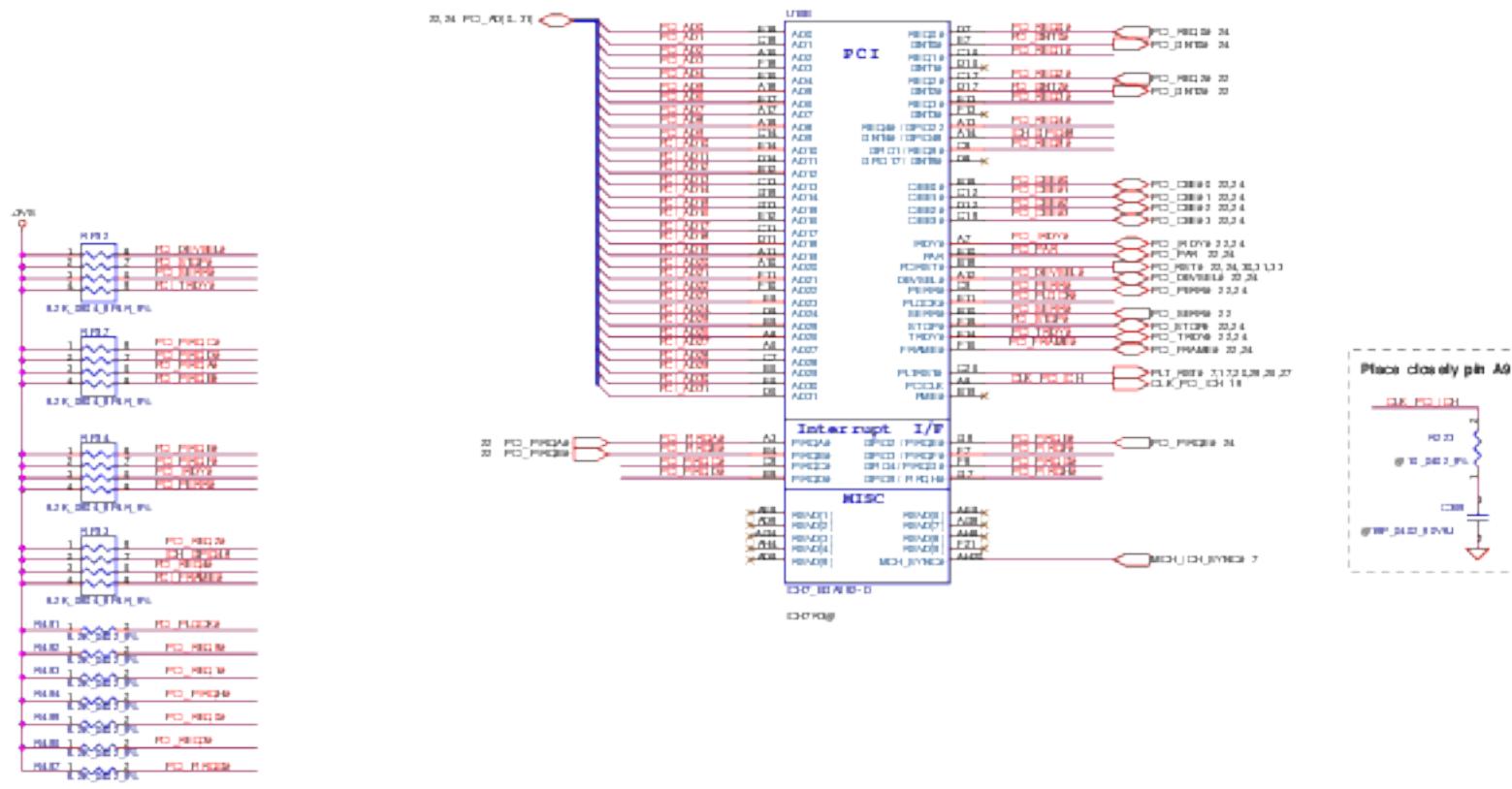
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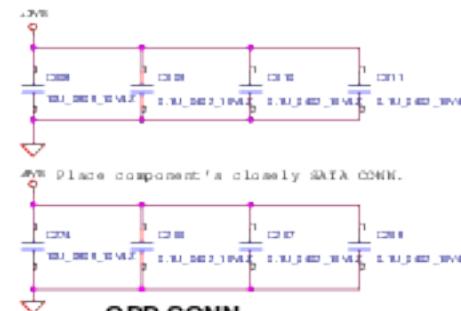
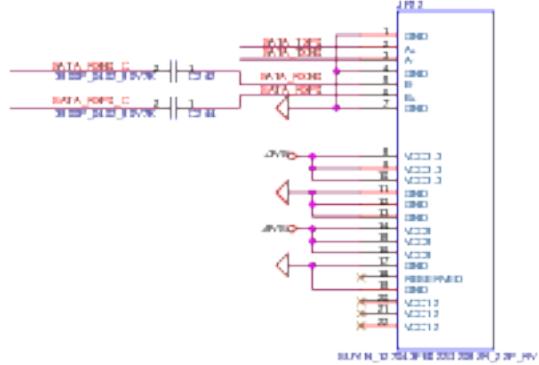
VGA / LCD CONN.

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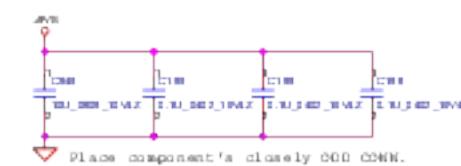
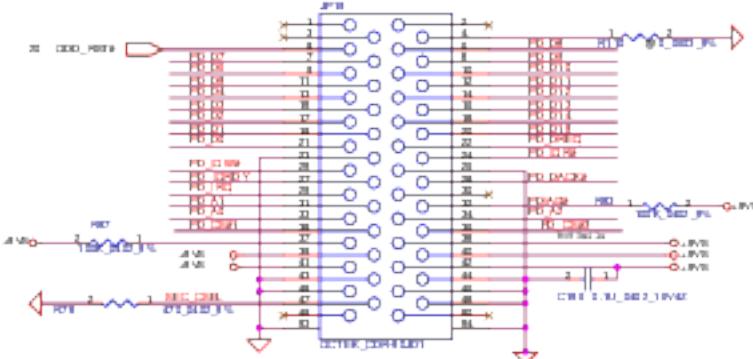
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File No.	Deciphered Date	Deciphered Date	Deciphered Date	Ref. No.	Rev. No.
File No.	Deciphered Date	Deciphered Date	Deciphered Date	Ref. No.	Rev. No.
File No.	Deciphered Date	Deciphered Date	Deciphered Date	Ref. No.	Rev. No.

SATA HDD CONN



ODD CONN

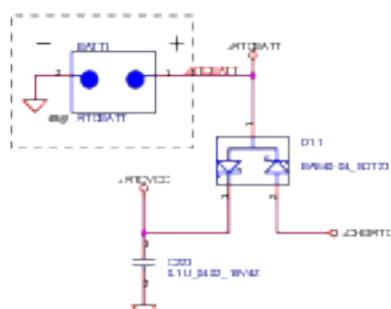
delete CD-Roms analog audio signal output



RTC Battery

Layout Note:

- Under BATT1 battery Body, no Trace no Via
- BATT1 + - PIN keep out 80mll from other component,trace and via



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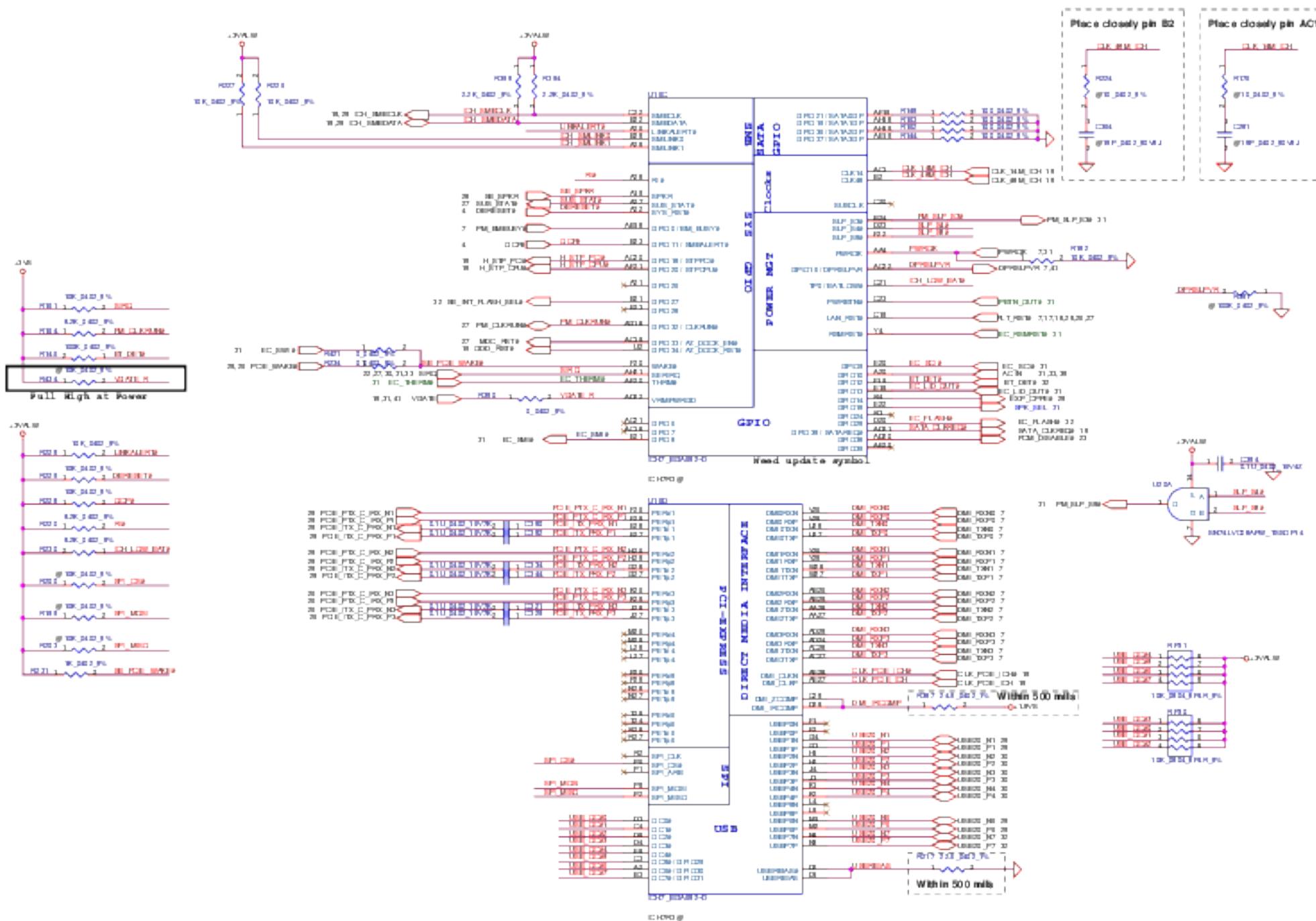
Compaq Electronics, Inc.

ICH7-M(2/4)

NT200 M/B LA-JTIP

Rev. Date and No. 000

Page 12



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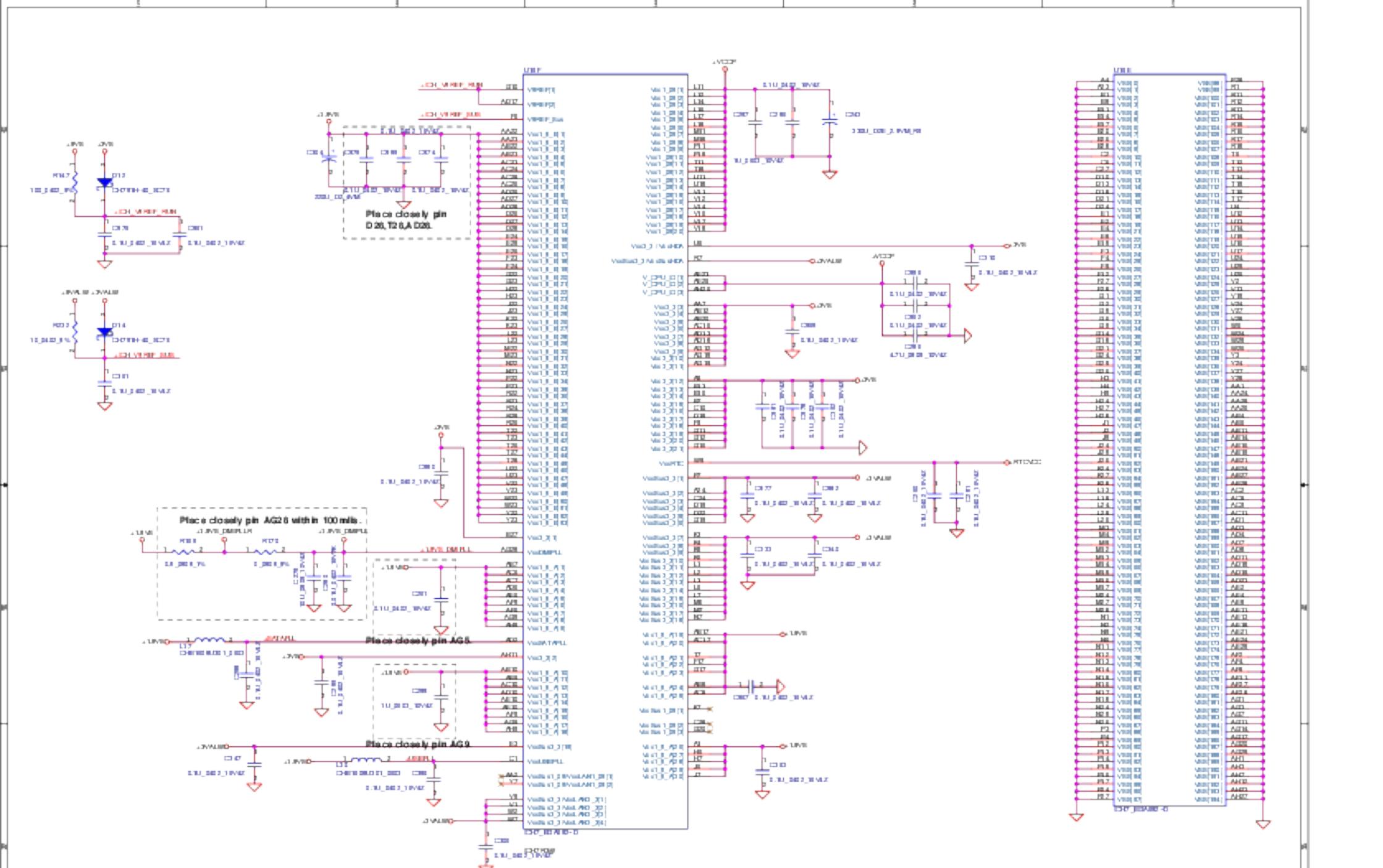
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NTW20 MIN LA-JTIP

Date: File No.: Page No.: Rev. No.: 1.0



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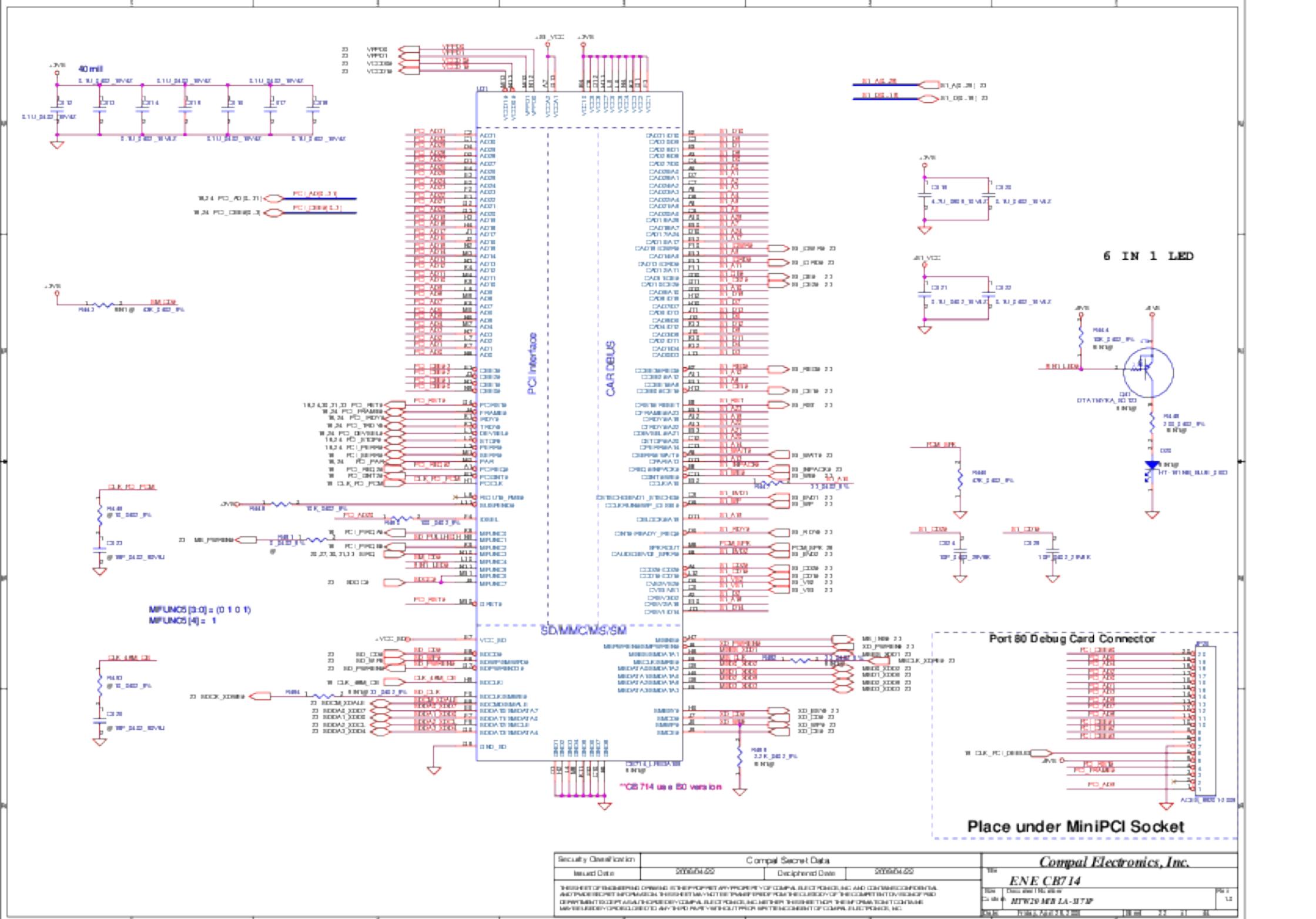
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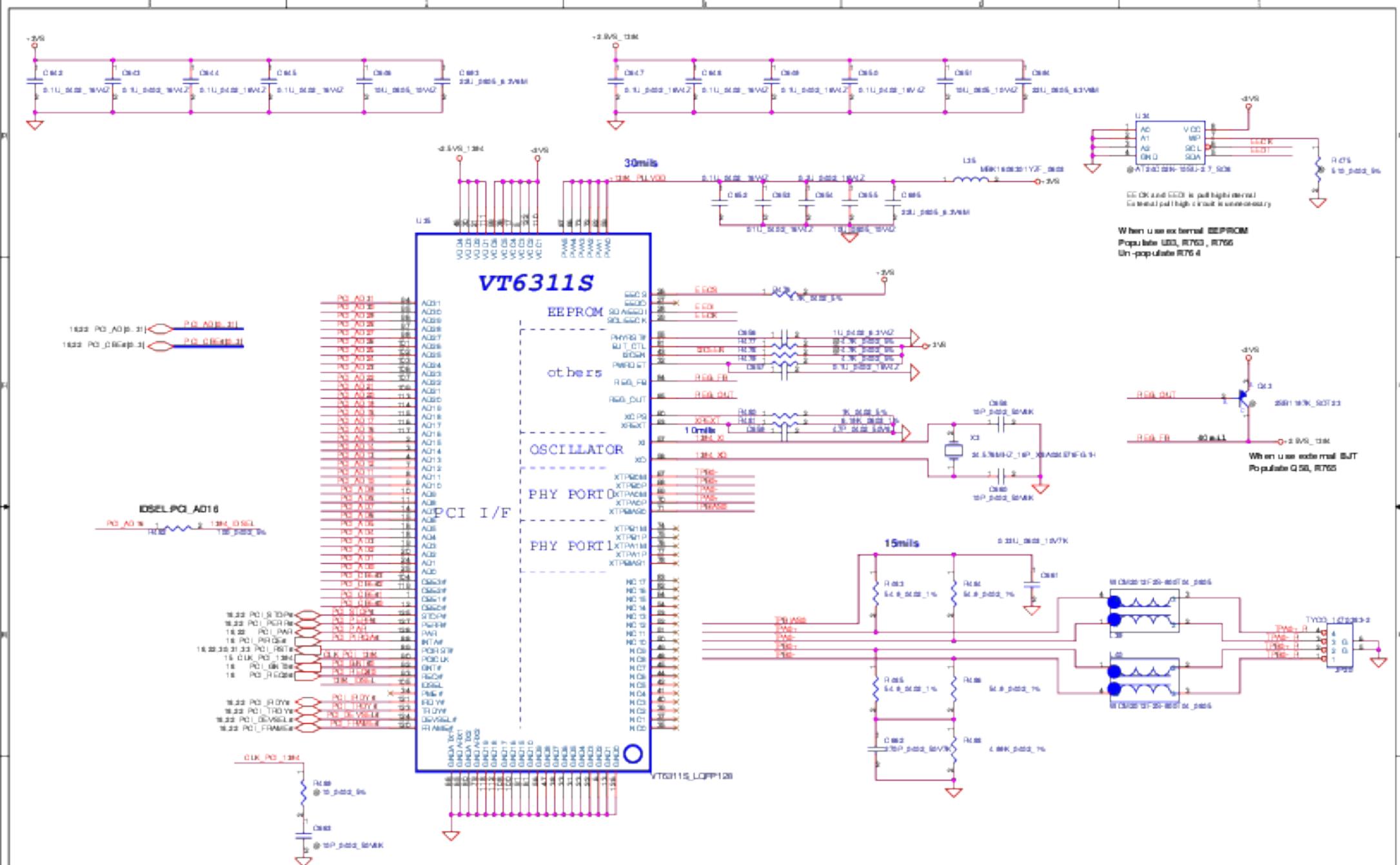
2009/06/22

2009/06/22

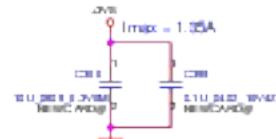
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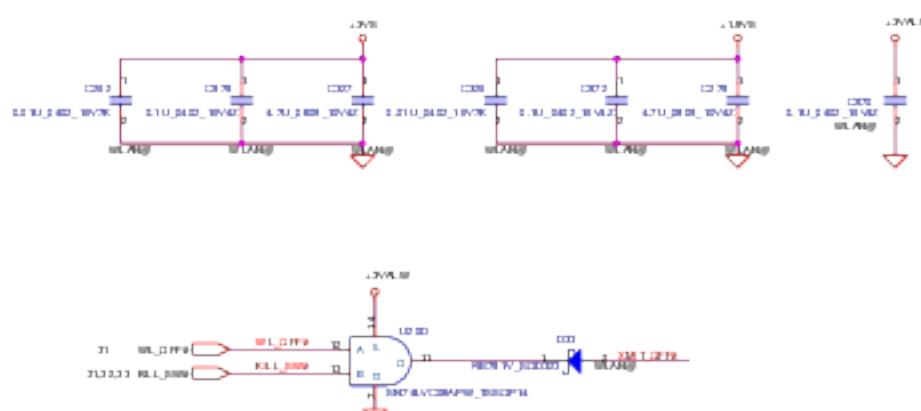
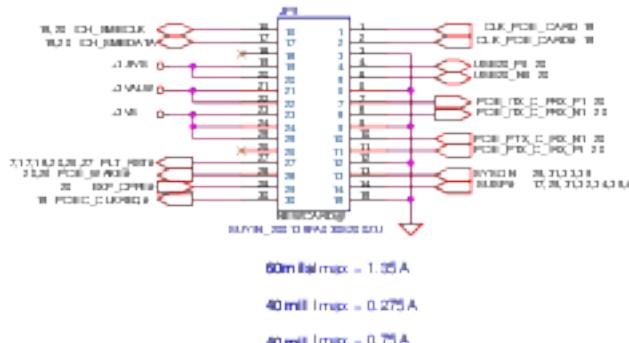




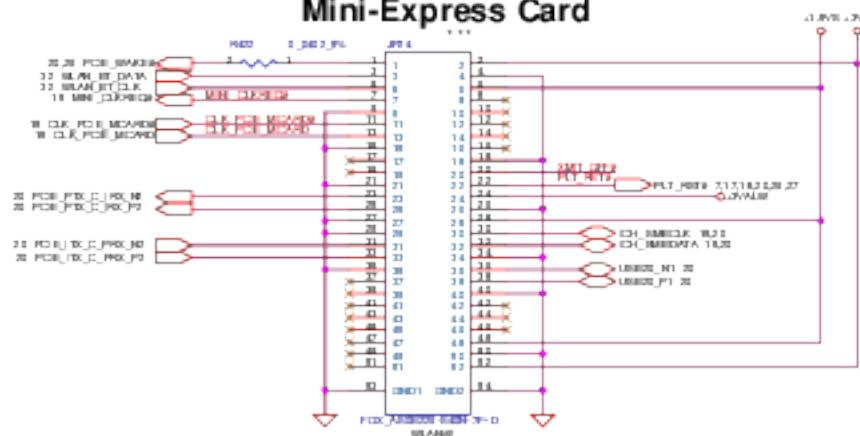
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2000/04/22	2000/04/22	IEEE1394 VIA VT6311S
2000/04/22	2000/04/22	Page A4/62



New Card Connector



Mini-Express Card



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2009/06/22 2009/06/22

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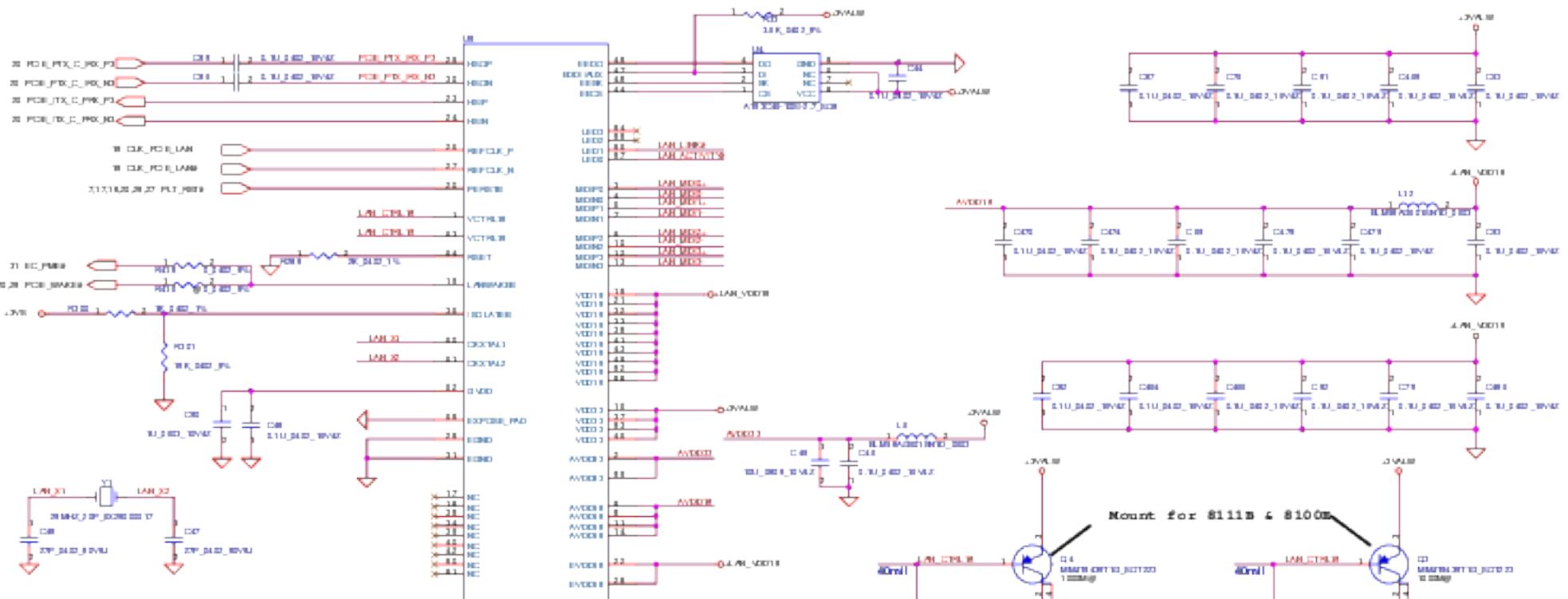
MinICard Conn & NewCard/B Conn

Rev. Date Issued Date 2009/06/22

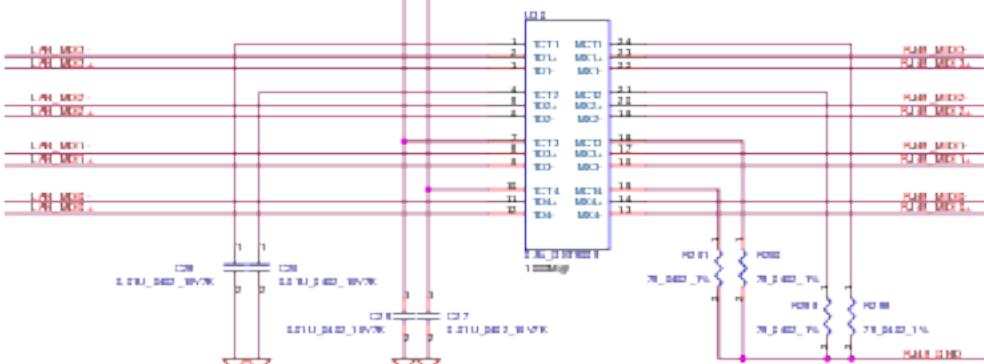
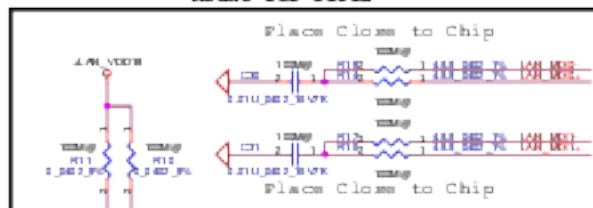
Ca date 1.2

Date 2009/06/22

Page 1 of 1



Mount for 8101E



Place these components
close to LAN chip

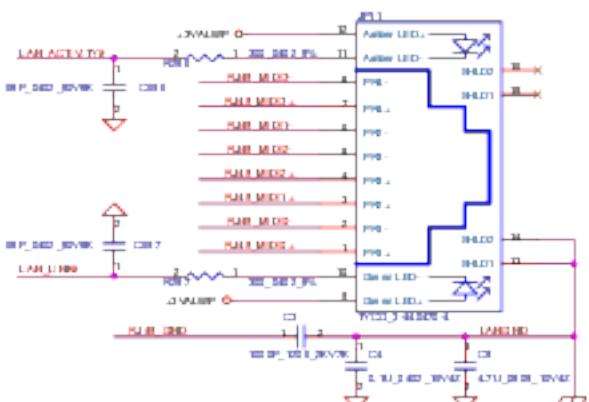
GST5009 for GIGA LAN
TST124 for 10/100 LAN

Mount for 8101E

Mount for 8101E



LAN Conn.



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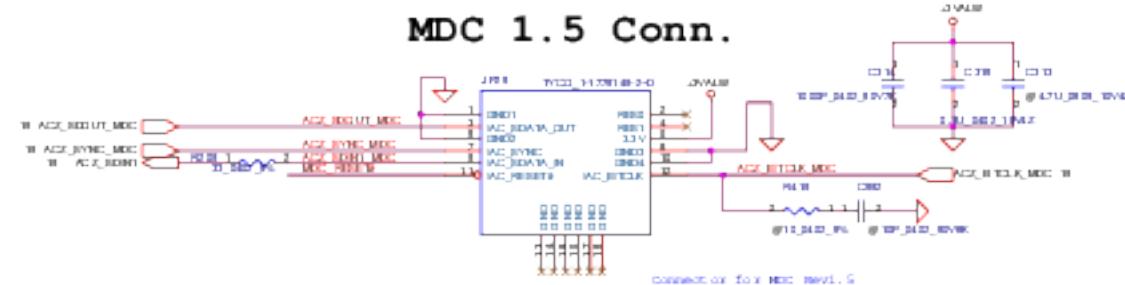
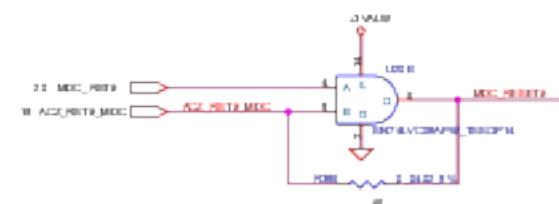
Compaq Electronics, Inc.

RTL8111B/8101E 10/100/1000 LAN

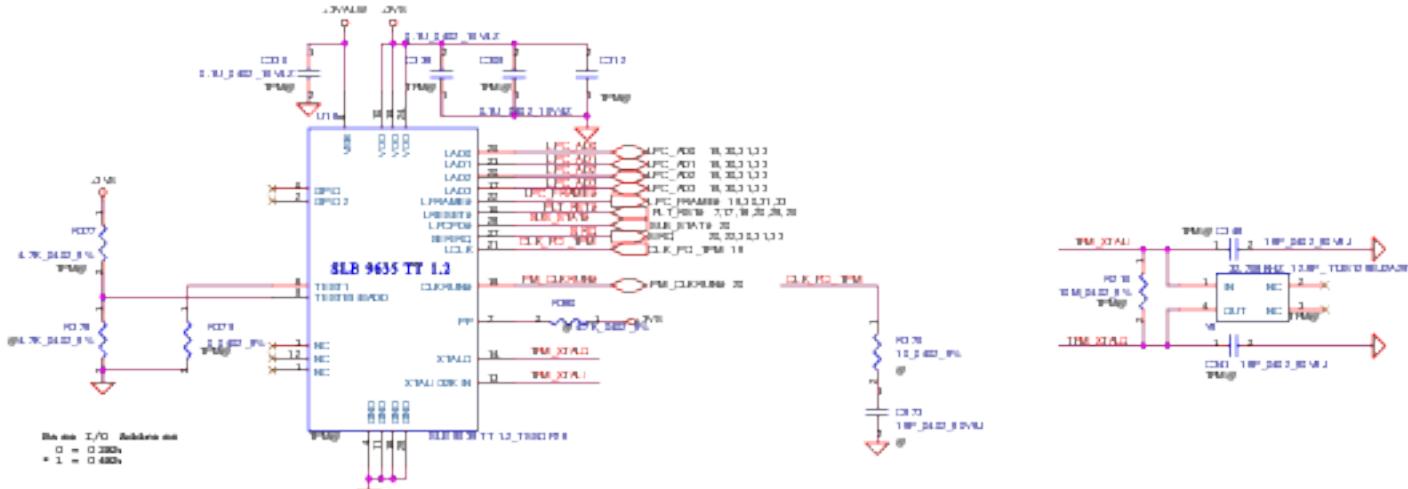
Rev. D, Decided Number:

C4-AW822-2-M01-LA-217P

Page 12

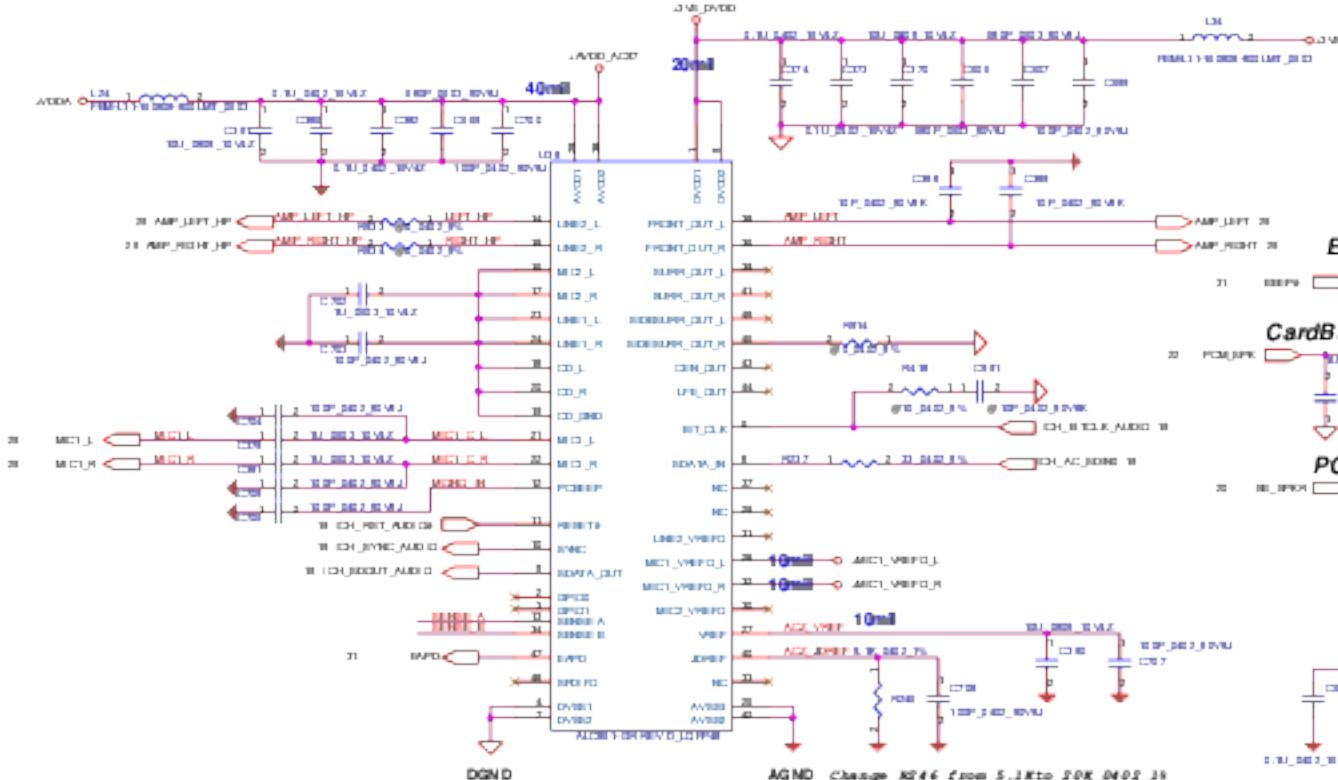


TPM1.2 on board

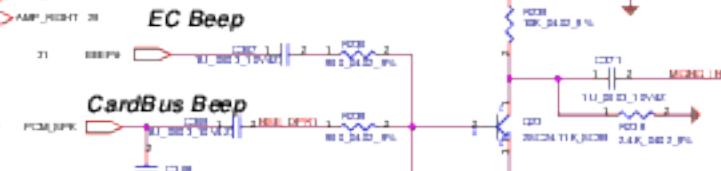


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Date	Deciphered Status	Rev	File No.	Page	Page
2009/01/22	OK	1.0	NTW20-MX-LA-JT1P	1.0	1.0

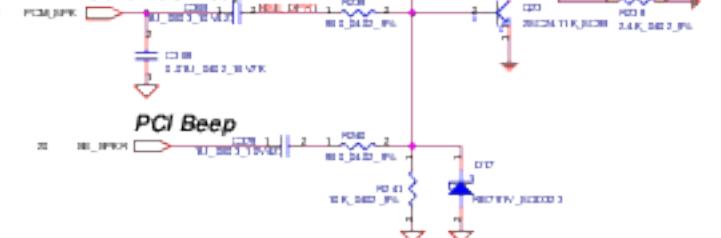
HD Audio Codec



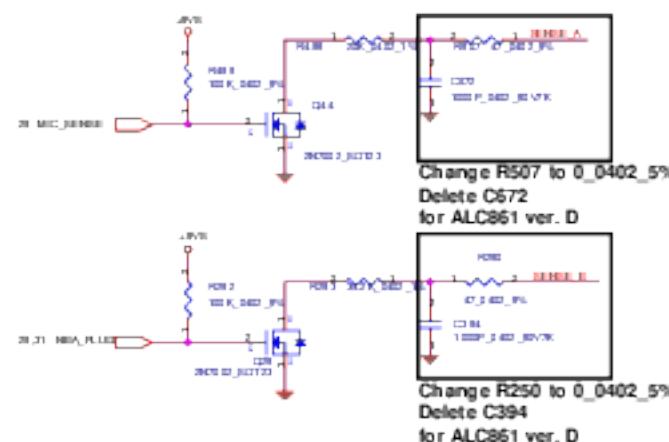
EC Beep



CardBus Beep



PCI Beep



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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20050420 20050420

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HID Audio Codec ALC861D

Rev. Date and Revision

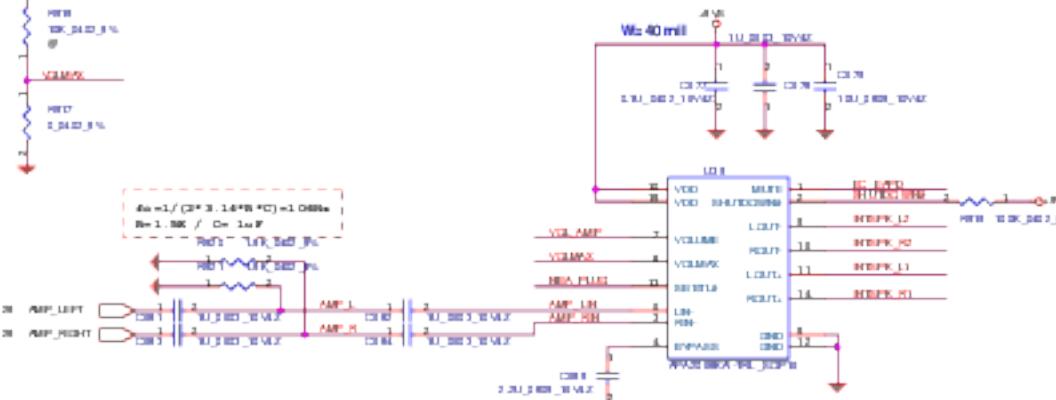
HTW20 M/B LA-3171 P

Page 1/2

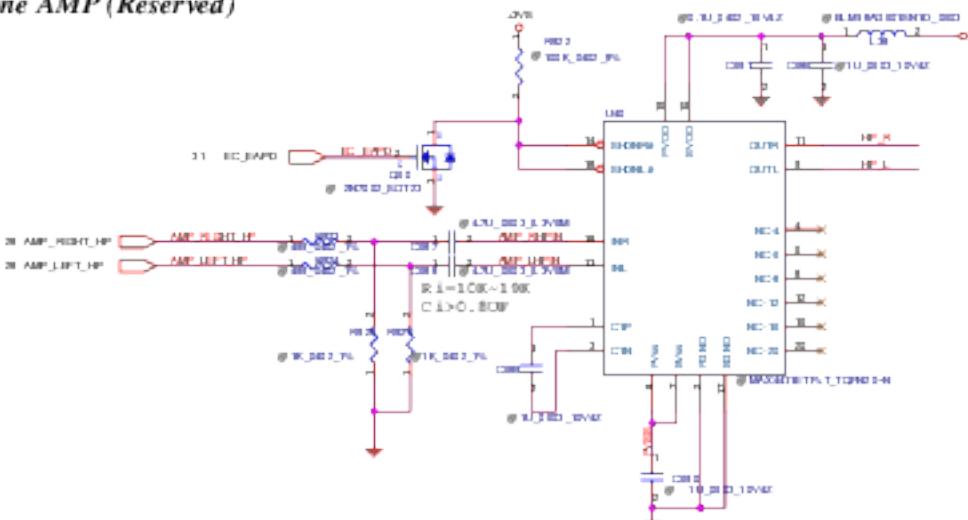
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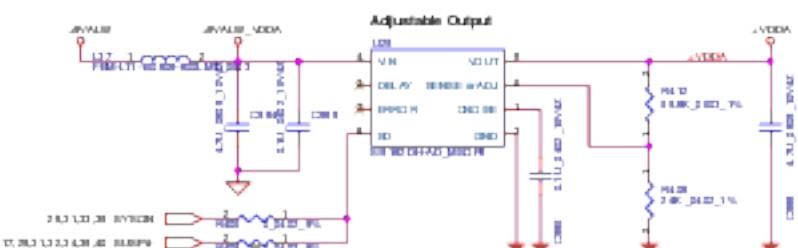
Speaker AMP



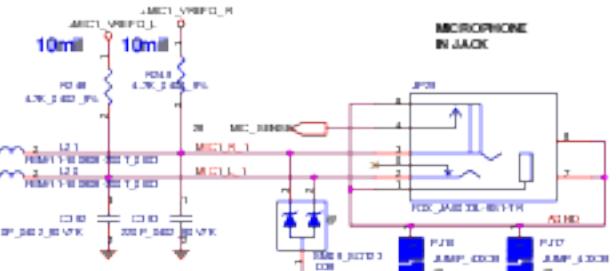
Headphone AMP (Reserved)



Regulator for CODEC

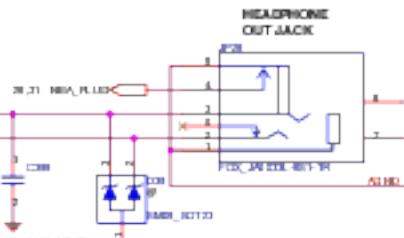


Moat Bridge

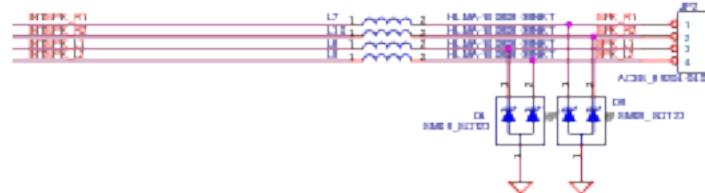


Microsoft Audio Hardware Design, Section "Analog Audio Classification Using Device Impedance"
Recommend: Audio Device Impedance:

Headset: 3.2 ~10.0 Ohm (C > 240 uF)
Passive Speakers: 4 ~160 Ohm (C > 1900uF)
Active Speakers: 3K ~15K Ohm (C > 2.65 uF)



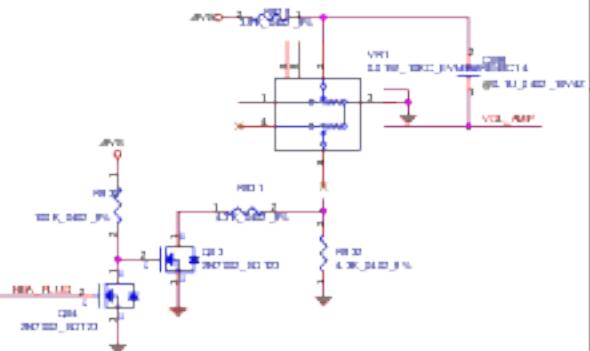
Speaker Connector



Gain Setting

	0dB	VOL AMP
SINK	1.0	0.66=3.7
SHP	0	1.18=3.9

Variable Resistor



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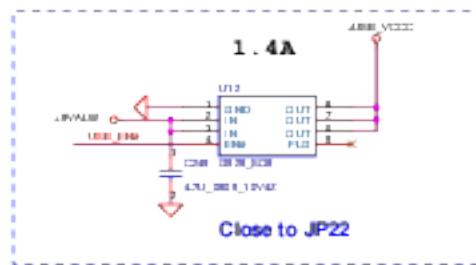
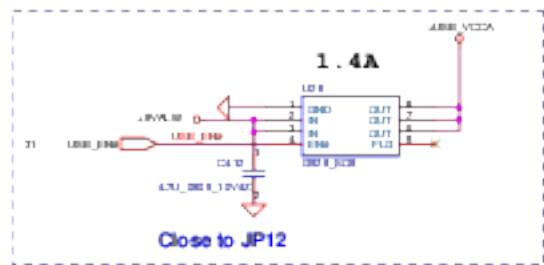
AMP/VR/Audio Jack

HTW20 M/B LA-3171P

Rev. 1.2

Date: 08/26/2004

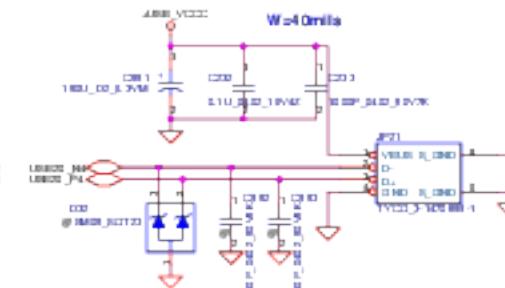
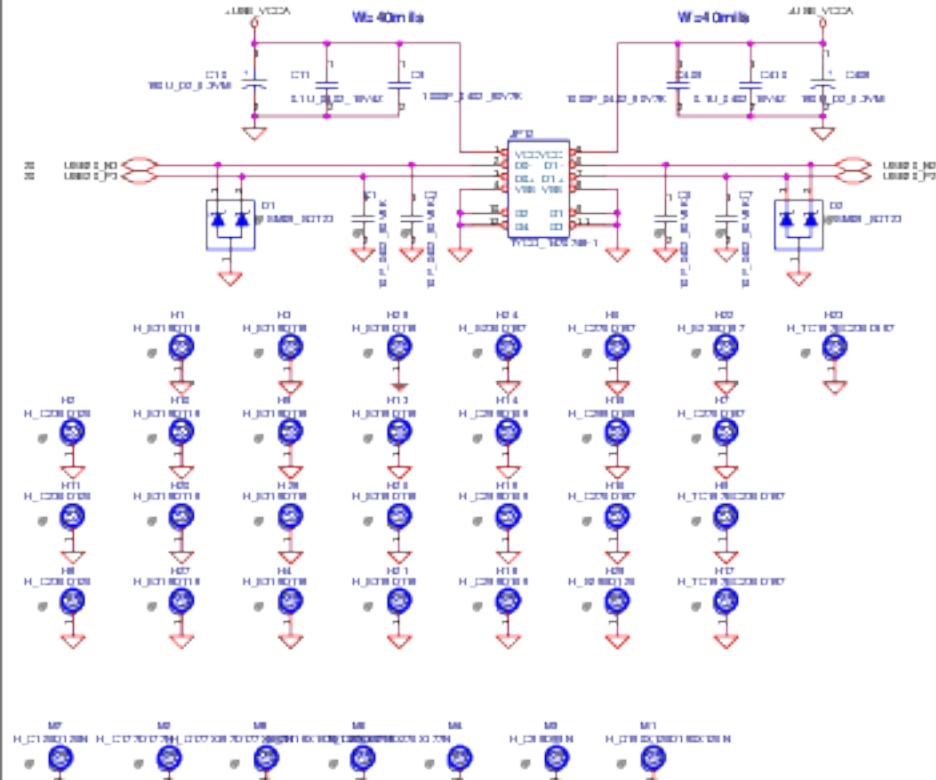
Page: 1/1



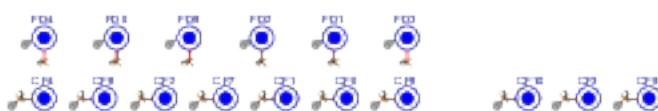
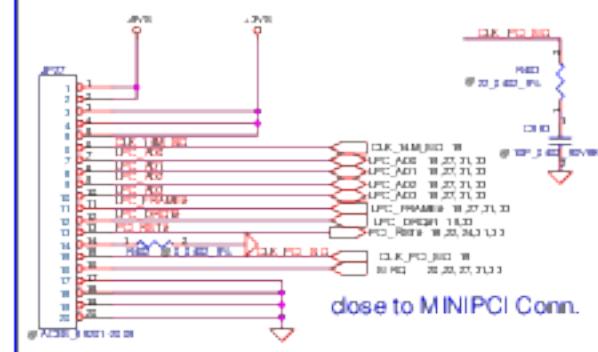
USB CONN. 1

USB CONN. 2

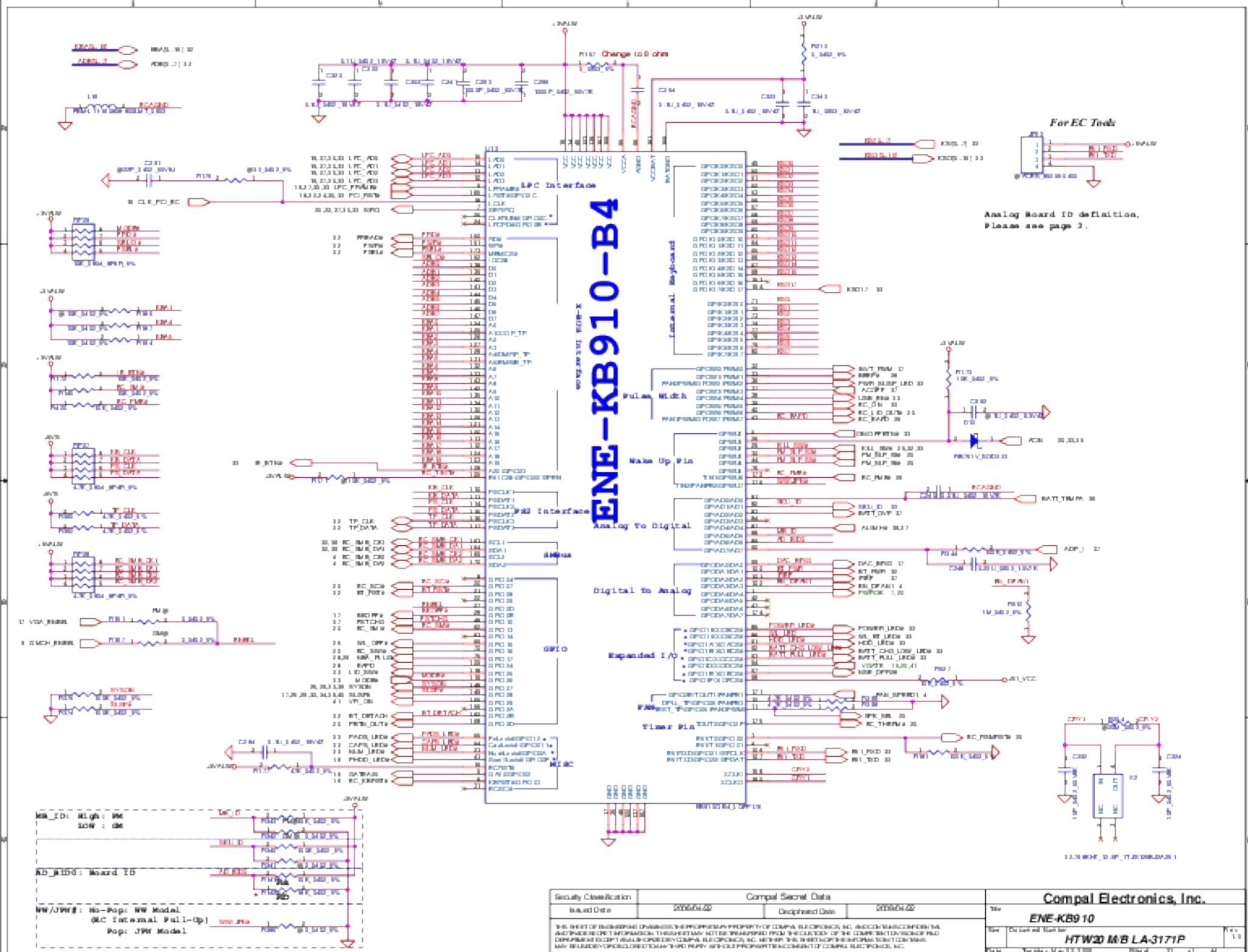
USB CONN. 3



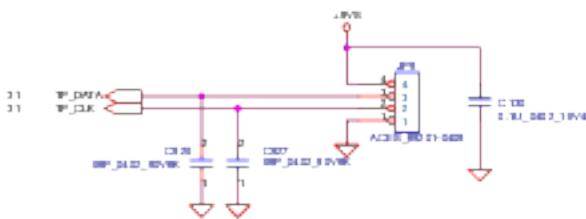
LPC Debug Port



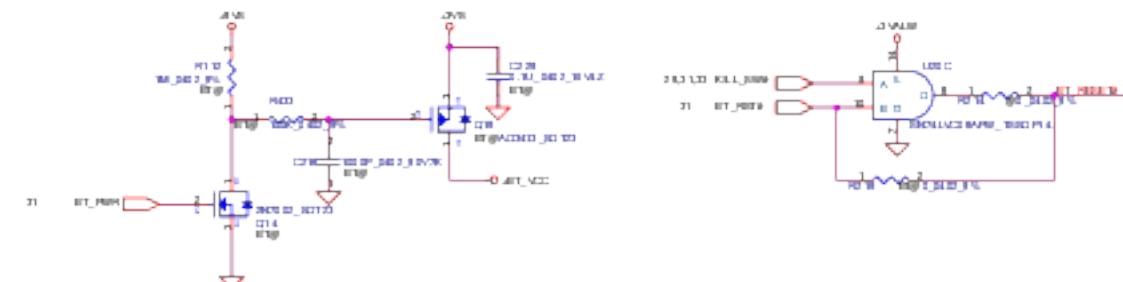
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	Deciphered Date	Title	Document Number
2009/06/20	2009/06/20	Screw Hole/USB/LPC Conn	HTW20M/B LA-3171 P
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2009/06/20	2009/06/20	Rev. 1.0	Page 12
F01 F02 F03 F04 F05 F06 F07 F08 PDS			



TP CONN.

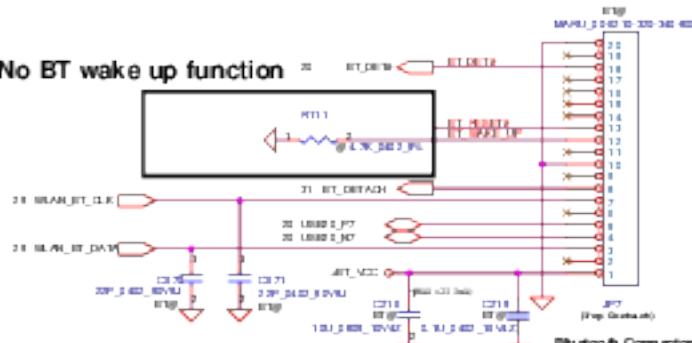


BlueTooth Interface

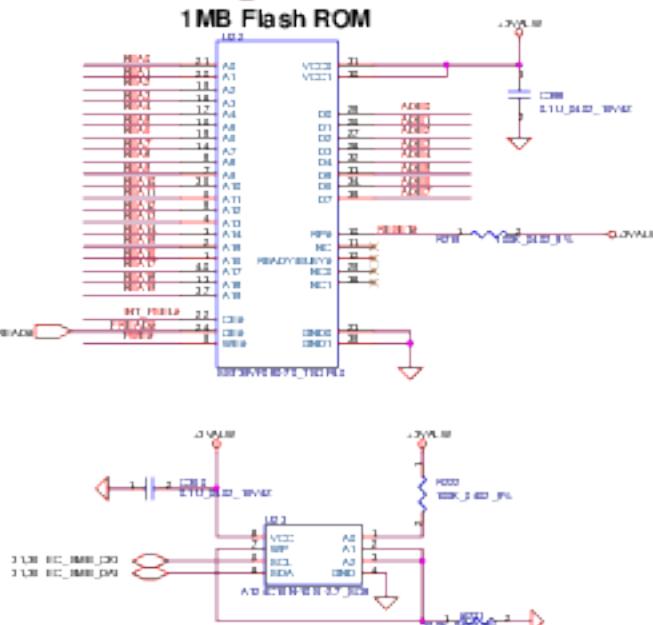


BT state ID:
Low level for pairing & Connect
High level for High Auto => Link;
Low level for Low Auto => Open

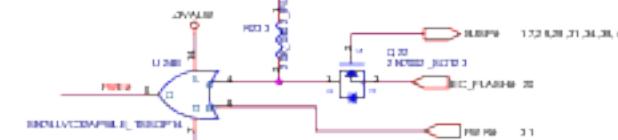
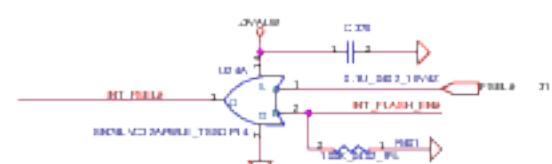
No BT wake up function



1MB Flash ROM



1MB ROM Socket



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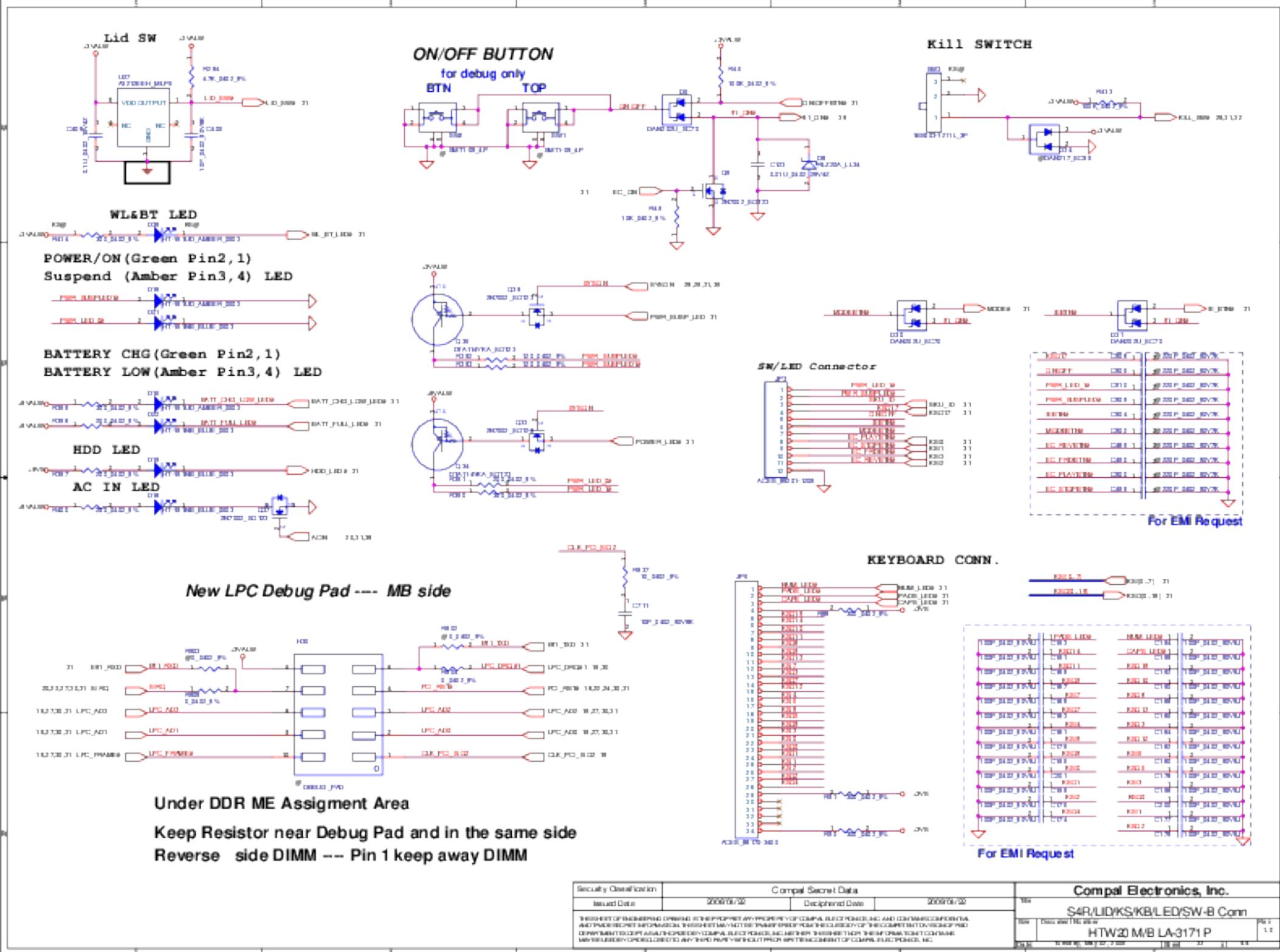
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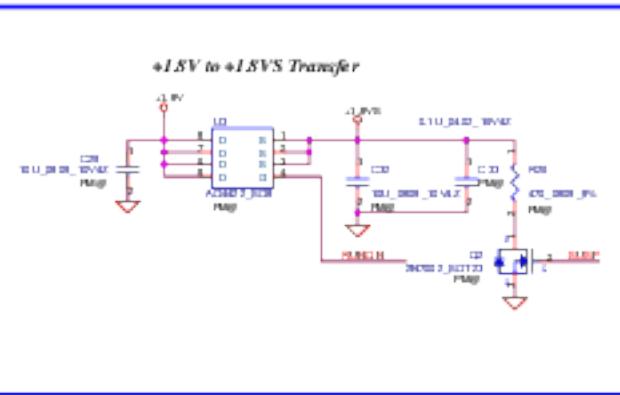
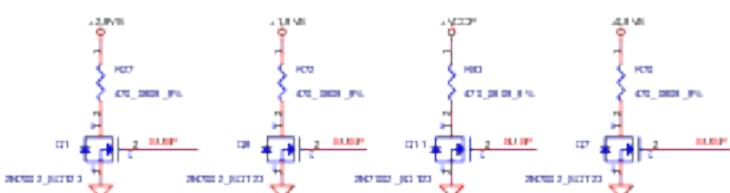
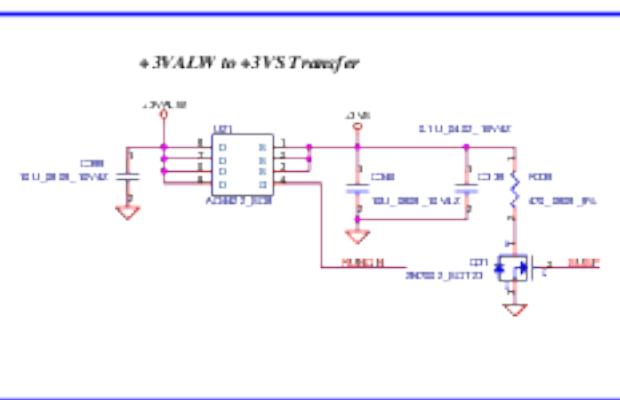
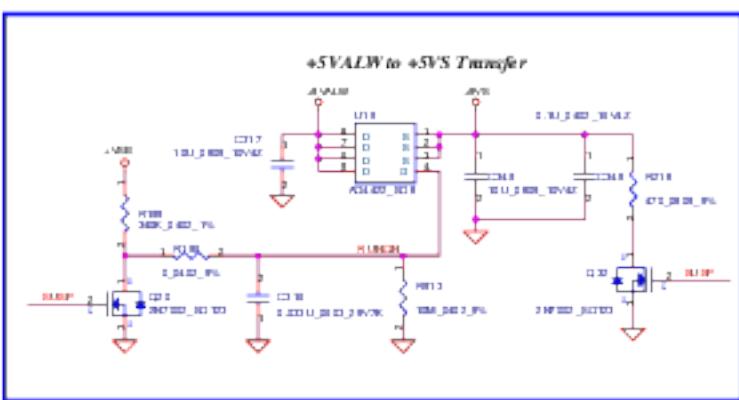
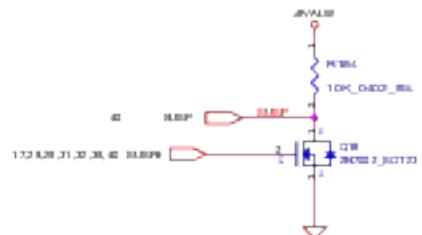
1MB BIOS/ TP Conn/ BT Conn

Rev: 1.0 Date Issued: 2009/04/22

HTW20 M/B LA-3171P

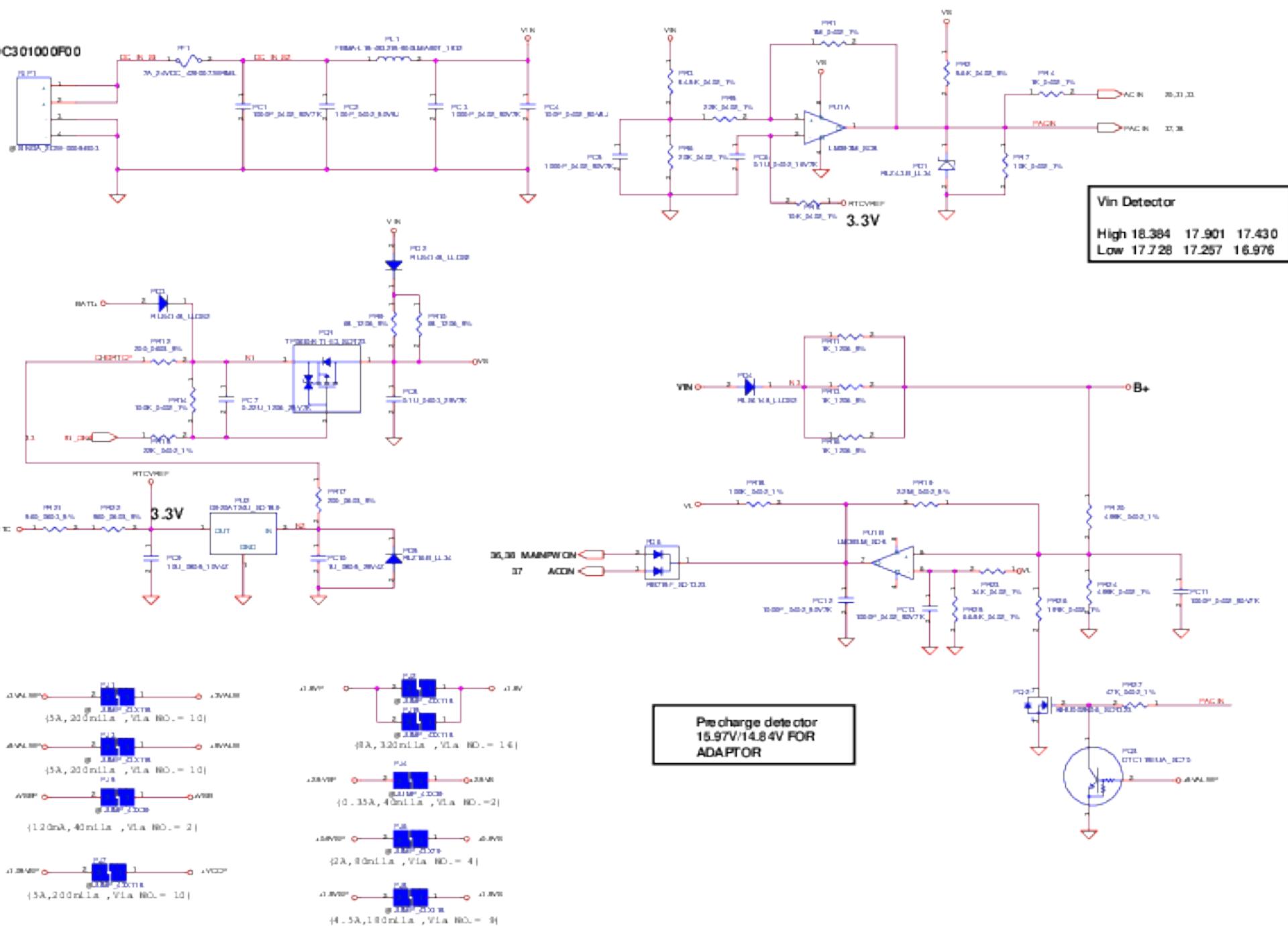
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Date Issued	File No.	Declassified Date	File No.	Rev.	Rev.
2009/06/22	MTW10 MIN LA-JTIP	2009/06/22	2009/06/22	1.2	1.2
Page	Page No.	Page No.	Page No.	Page No.	Page No.
1	1	1	1	1	1

DC30100 OF00



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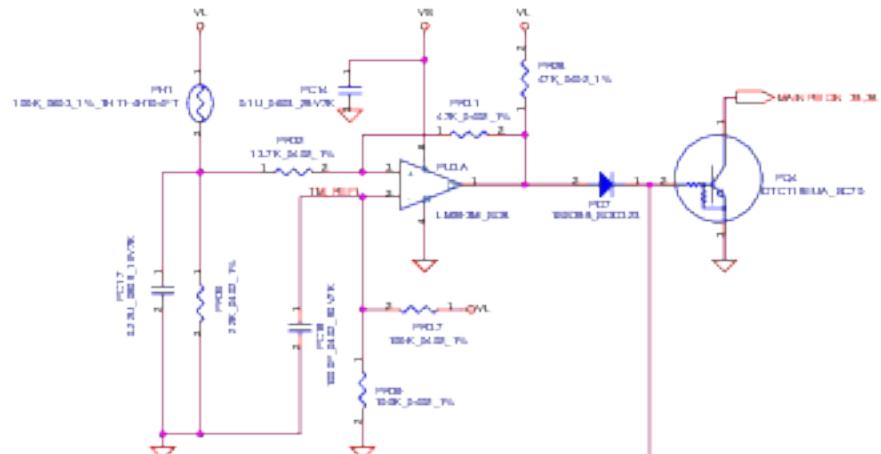
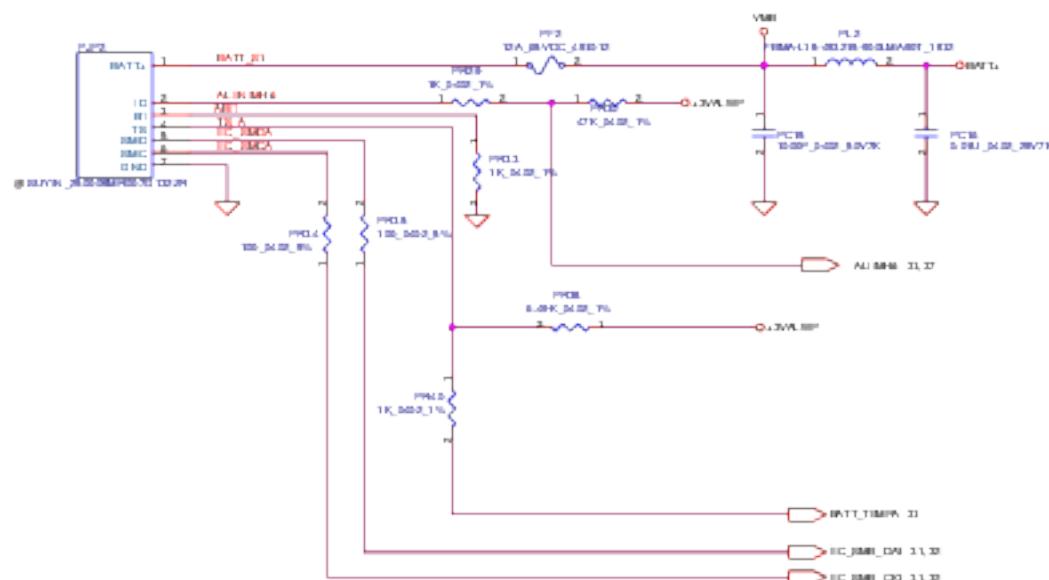
DCIN & DETECTOR

Date Issued/Revised

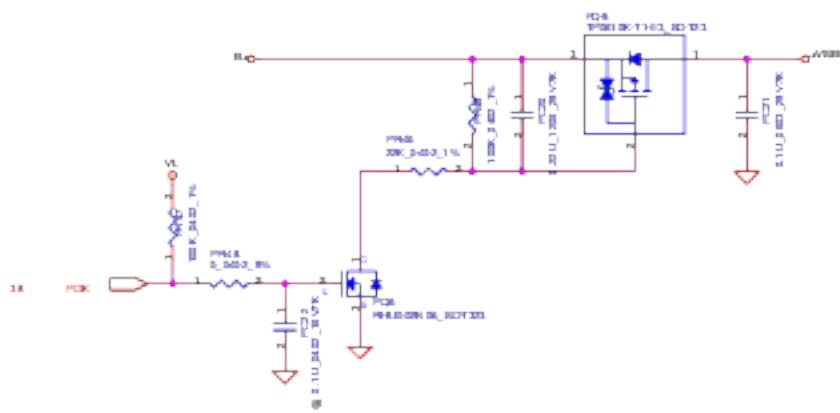
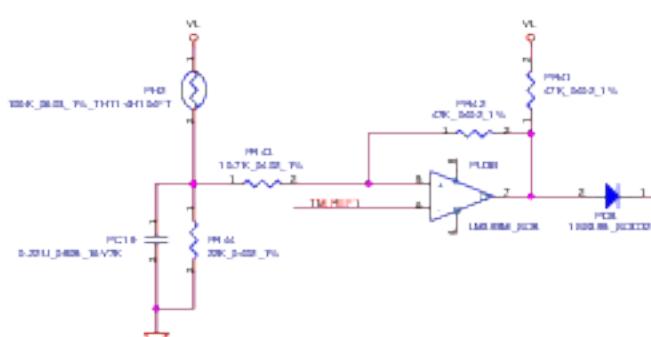
Page

1/1

PH1 under CPU bottom side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



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Issued Date

Declassify Date

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2009/06/22

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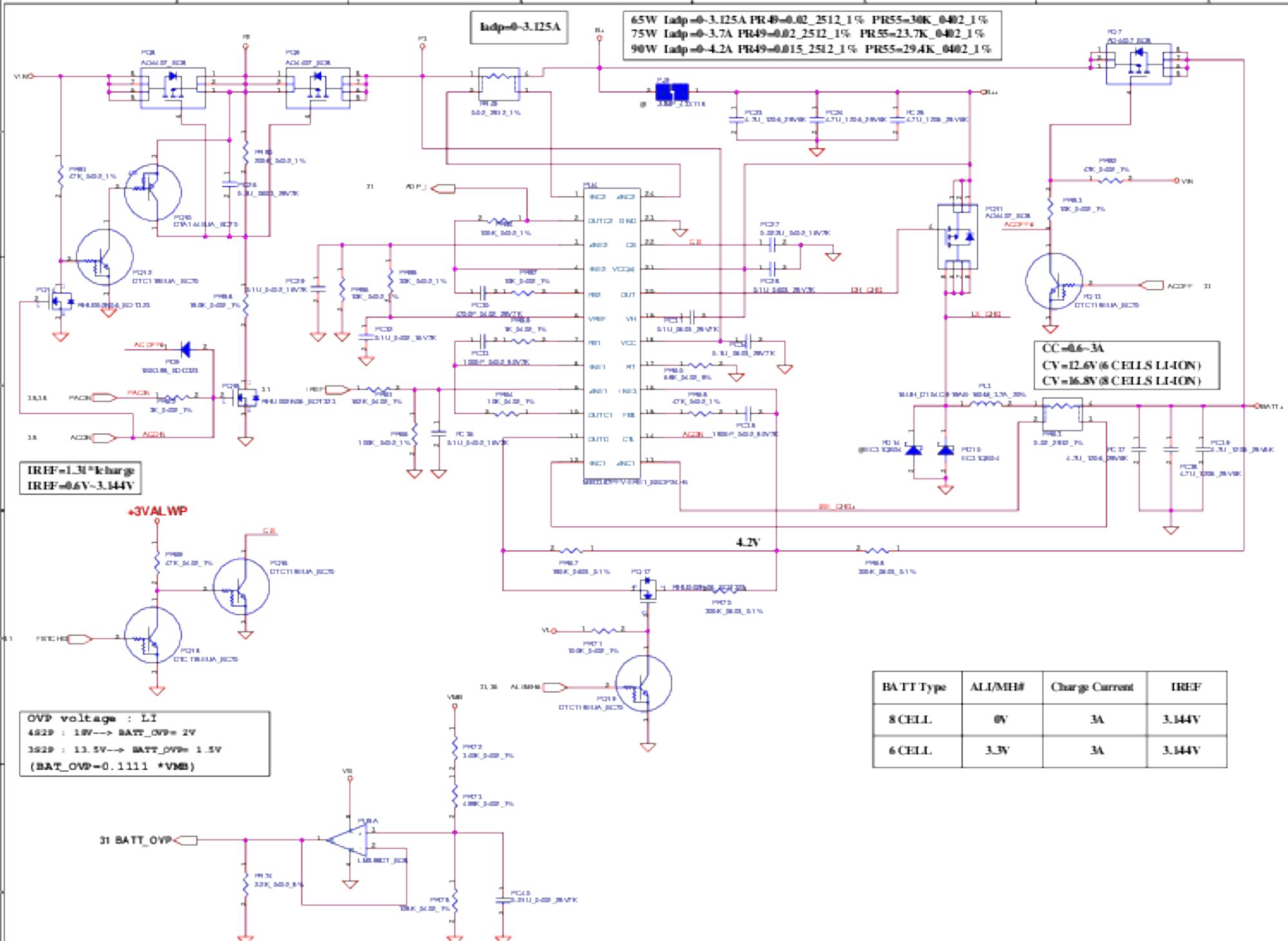
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BATTERY CONN / OTP

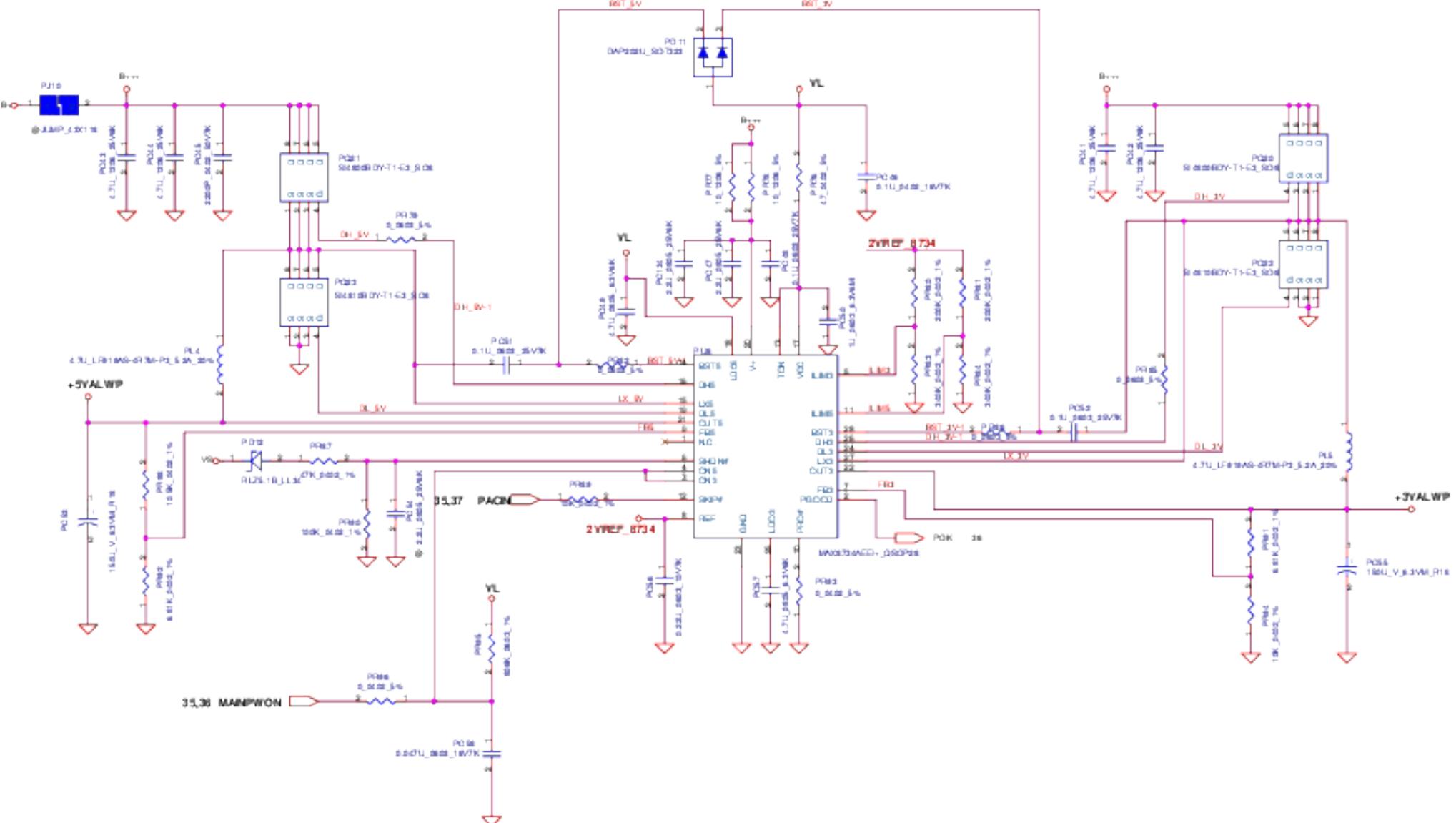
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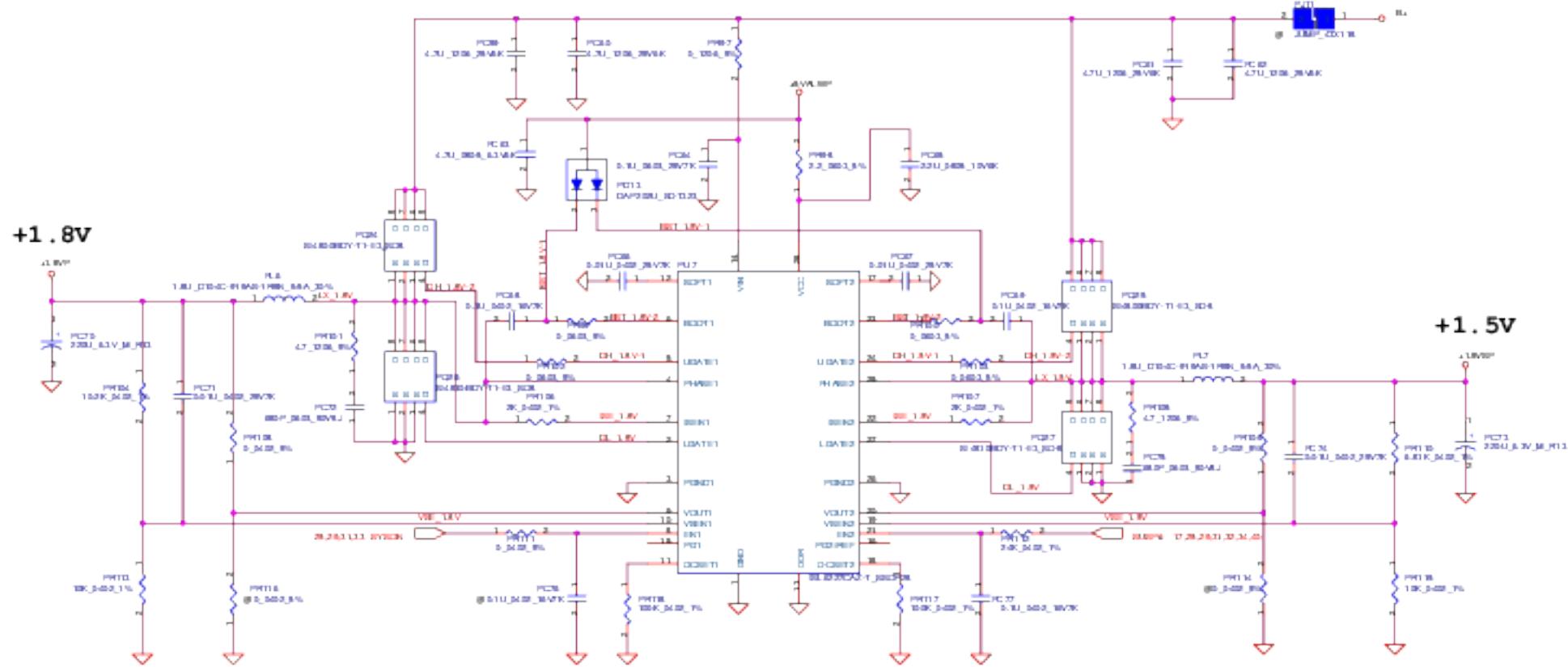
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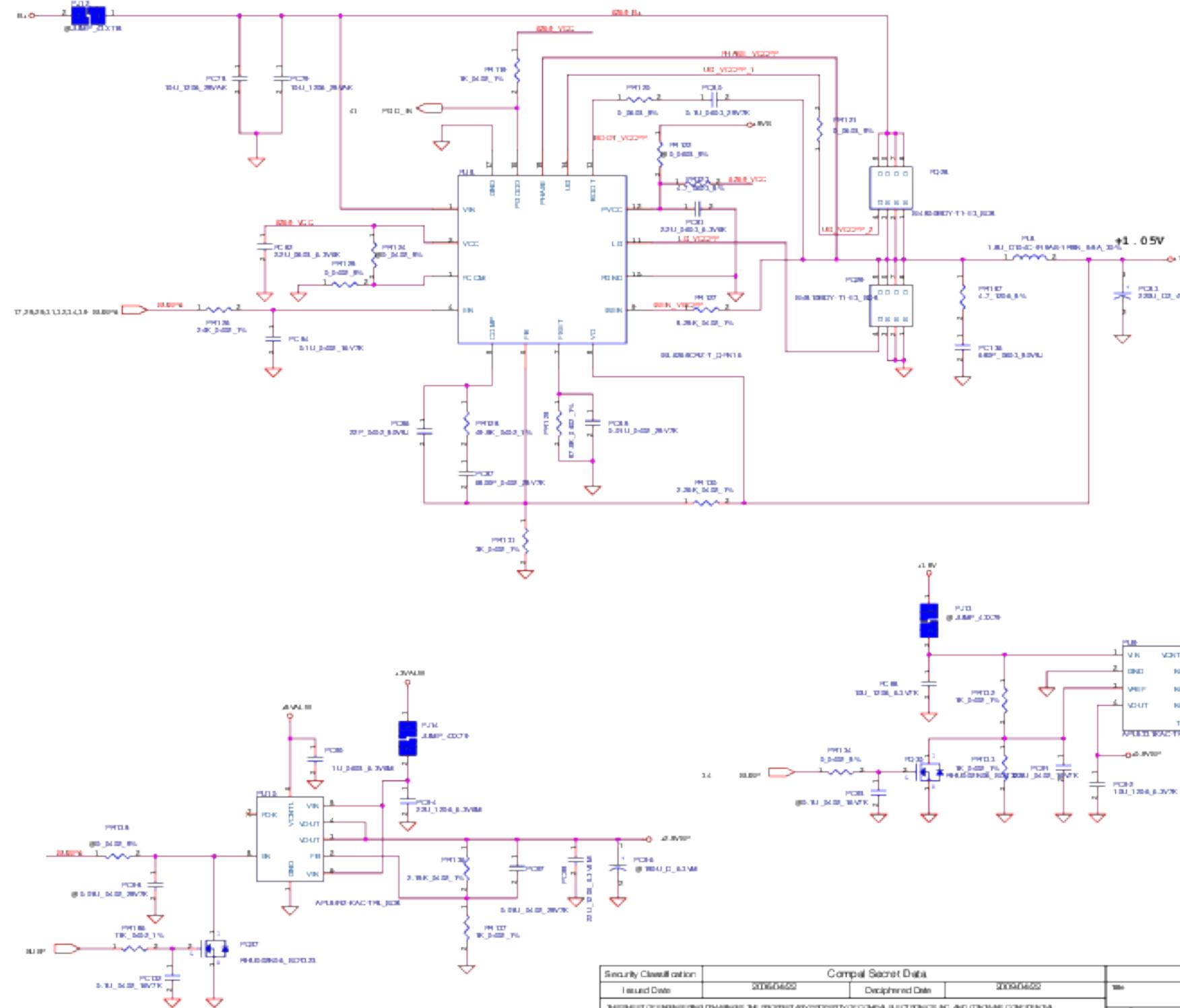
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2000/04/22	2000/04/22	+5V/+3V
2000/04/22	2000/04/22	HTW20MB LA-317IP
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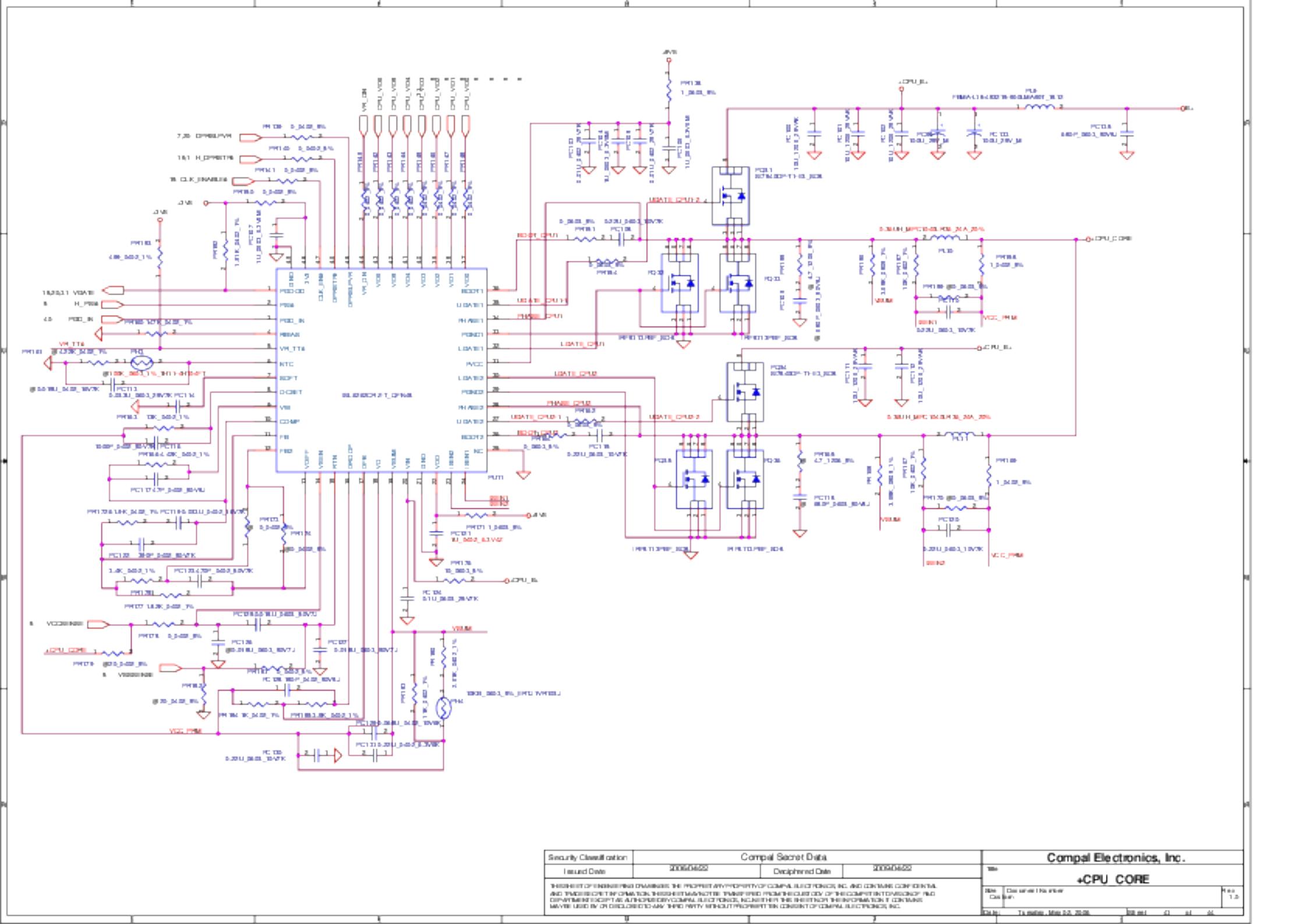
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POWER PIR LIST

page Reason for change

Modify list

EVT->DVT	
40	Add 680P at B+ for ENI
38	Change 1.5V sequence for BM
39	Change 2.5V sequence for BM
39	Change 2.5V sequence for BM
38	Adjust 3V/5V OCP to 8A
41	Adjust CPU loadline
	Modify list
	Add 680P_0402_25V at B+
	Change PR112 from 22K_0402_1% to 24K_0402_1%
	Unpop PR135, PC98 Pop PR186=11_K0402_1%, PG37, PC132=0.1u_0402_16V
	Change PR104 from 10K_0402_1% to 10.2K_0402_1%
	Change PR80, PR81 to 200K_0402_1%, PR83, PR84 to 340K_0402_1% , PL4, PL5 to 4.7uH
	Change PC119 to 33u_0402_16V, PR185 to 3.9K_0402_1%

DVT->PVT

40	Add snubber at 1.05V	Add 4.7_1206_5% and 680P_0603_50V at PR187,PC136
41	Adjust switching frequency for interval suggest	Change PC117 from 5600P to 47P_0402_50V Change PR166 from 3.57K to 4.42K_0402_1%
40	Adjust 1.05 OCP to 8A	Change PR127 from 11.5K to 8.25K_0402_1%

PR104/112/120				Compel Secret Data				Compel Electronics, Inc.		
Security Classification	Issued Date	Declassified Date	Ref	Ref	Declassified Date	Ref	PIR	Ref	Declassified Date	Ref
REF ID: PIR-104-112-120	2009/04/22	2009/06/22	PR104	PR112	PR120	PR120	PR104	PR112	PR120	PR104

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HW4 Product Improvement Record (P.I.R.)

Phase: A to B		Date: 2006/01/04			Writer: Lion Wang		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
22,23	none	none			change TI8412 to ENK 714 for CB & 5in1 function	0.2	
24	none	none			change TI8412 to VIA6311S for 1394 function	0.2	
28	Add	C606,C607			Add for EMI request	0.2	
28	Add	L32			Add for EMI request	0.2	
31	Unmount	R171,R185			update after check ENK FAE	0.2	
31	Change	R365,R368 R187,R194	1K_5%_0402	10K_5%_0402	update after check ENK FAE	0.2	
31	Change	L33	Bead	0_5%_0603	update after check ENK FAE	0.2	
19	Change	JP22			change HDD CONN.	0.2	
31	Change	R142	0_5%_0402	8.2K_5%_0402	update BID from REV0.1 to REV0.2	0.2	
29					change U27,D38 ,D39 connect from GND to AGND	0.2	
26	Del	L33			LMW PCIE detect issue cause system boot black screen	0.2	
29	Change	SW4			Change VR to Rock Type switch	0.2	
29	Change	R514,R517,R516			Change AMP HP gain from -6 dB to 0 dB	0.2	
28	Add	Q44,R507,R498 C672,R499			Add for MIC Jack present function	0.2	
26	Change	R10,R11			change R10,R11 connect to U30 PIN7 & PIN10 to fix 10/100 Lan cannot connect issue	0.3	
20	Change				change ODD_RST# from GPIO 24 to GPIO34	0.3	
24	Change				delete R508-R511 and add L39 & L40 for EMI request	0.3	
						0.3	

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	Deciphered Date	Deciphered Date	Deciphered Date	PIR	PIR	PIR
2006/01/04	2006/01/04	2006/01/04	2006/01/04	PIR	PIR	PIR
				MTW20 MINI LA-STIP		Rev. 1.1
				00000000000000000000000000000000		

HTW20 LA-3171P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 0.4

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	LAN	TRANSFORMER	PCB	Card BUS	SB	NB	LB	LB
1	0327	29	REMOVE C680,R516,R518 REMOVE SW4 REMOVE CONNECTION OF VOL_UP,VOL_DOWN,VOL_MUTE,KSO17 ADD CONNECTION OF NBA_PLUG ON U39.13 ADD R529_3.9K_0402_5%,R530_100K_0402_5%,R531_4.3K_0402_5% R532_4.3K_0402_5%,Q62,Q63 RESERVE C698_0.1U_0402	MODIFY VOL_AMP FUNCTIONAL CIRCUIT ADD VR CIRCUIT								
2	0327	28	RESERVE R533 CONNECT BETWEEN AMP_LEFT_HP & LEFT_HP RESERVE R534 CONNECT BETWEEN AMP_RIGHT_HP & RIGHT_HP 29 ADD R535 CONNECT BETWEEN INTSPK_R1 & AMP_RIGHT_HP ADD R536 CONNECT BETWEEN INTSPK_L1 & AMP_LEFT_HP	MODIFY EARPHONE GAIN CONTROL CIRCUIT								
3	0327	28	ADD C699_100P_0402 ON +3VS_DVID ADD C700_100P_0402 ON +AVDD_AC97 ADD C702_1U,C703_100P ON U38 PIN 16,17,18,19,20,23,24 ADD C704_100P_0402 ON MIC1_C_L ADD C705_100P_0402 ON MIC1_C_R ADD C706_100P_0402 ON MONO_IN ADD C707_100P_0402 ON ACZ_VREF ADD C708_100P_0402 ON ACZ_JDREF ADD C709_100P_0402 ON +MIC1_VREPO_R ADD C710_100P_0402 ON +MIC1_VREPO_L	FOR EMI PURPOSE								

HTW20 LA-3171P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.4 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	0417	33	ADD R537_10_0402 AND C711_10P_0402 ON CLK_PCI_SI02	PREVENT PCI CLOCK TRACE FLOATING
2	0419	16	CHANGE L26,L25 TO 39_0402 CHANGE C411,C413 TO RESERVED	BASE ON INTEL CRB SCHEMATIC TO IO MODIFICATION (CRB REV:1.601)
3	0419	29	CONNECT VR1.1,VR1.2 TO AGND	BASE ESD TEST RESULT, CONNECT TO AGND TO PASS ESD TEST
4	0419	29	CHANGE L7,L8,L9,L10 TO BEAD 390HN@100MHZ CHANGE C395,C399 TO 10P_0402 28 CHANGE C388,C389 TO 10P_0402	TO SOLVE 3G NOISE ISSUE
4	0426	06	Add C122,C537 to 330UF	TO SOLVE ESD ISSUE