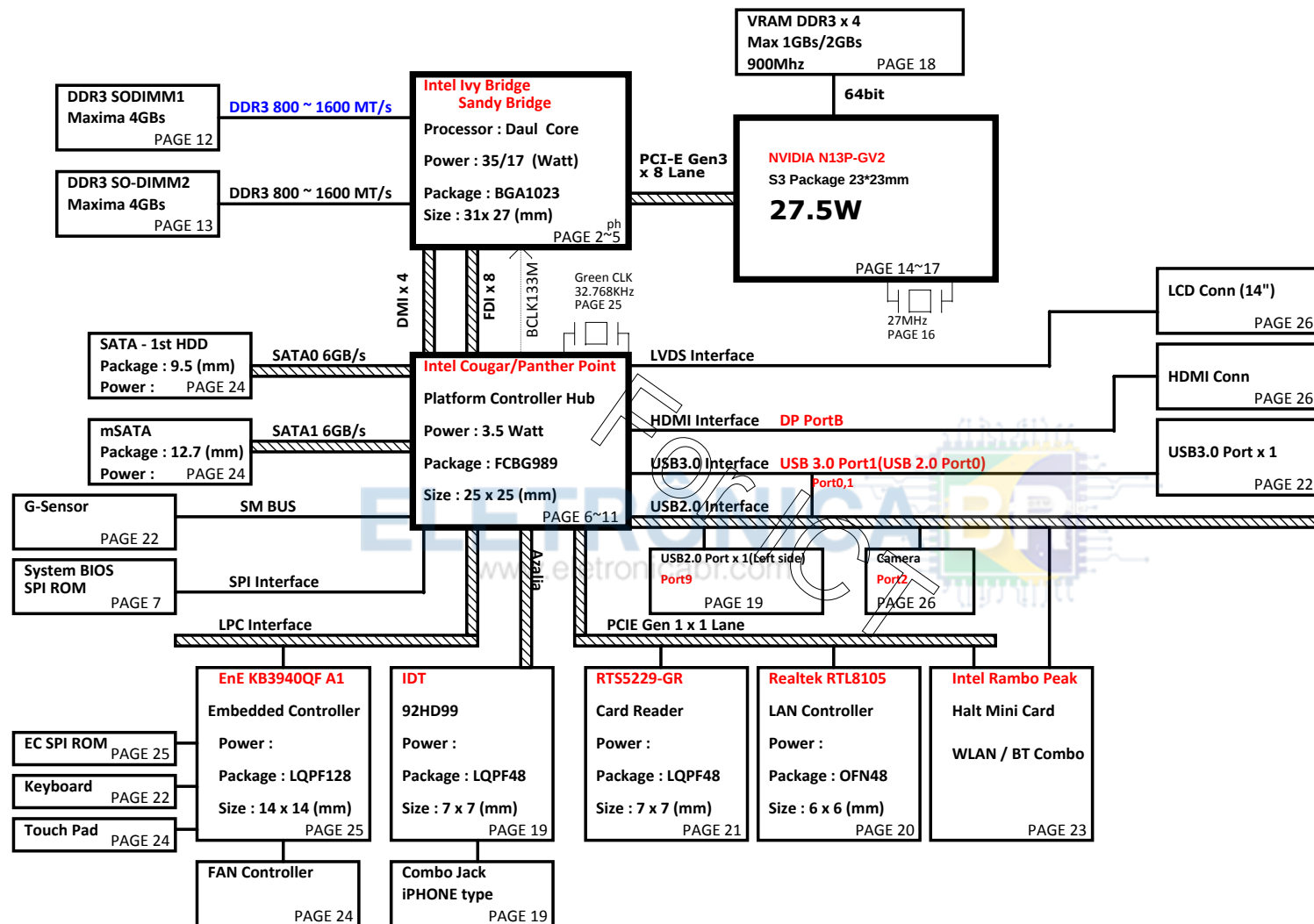


Volks DIS/UMA (14"/15.6") Ultra/Slim Intel Chief River Platform Block Diagram



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24738
System Charge Power (+BATCHG)

Ricktek RT8223P
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

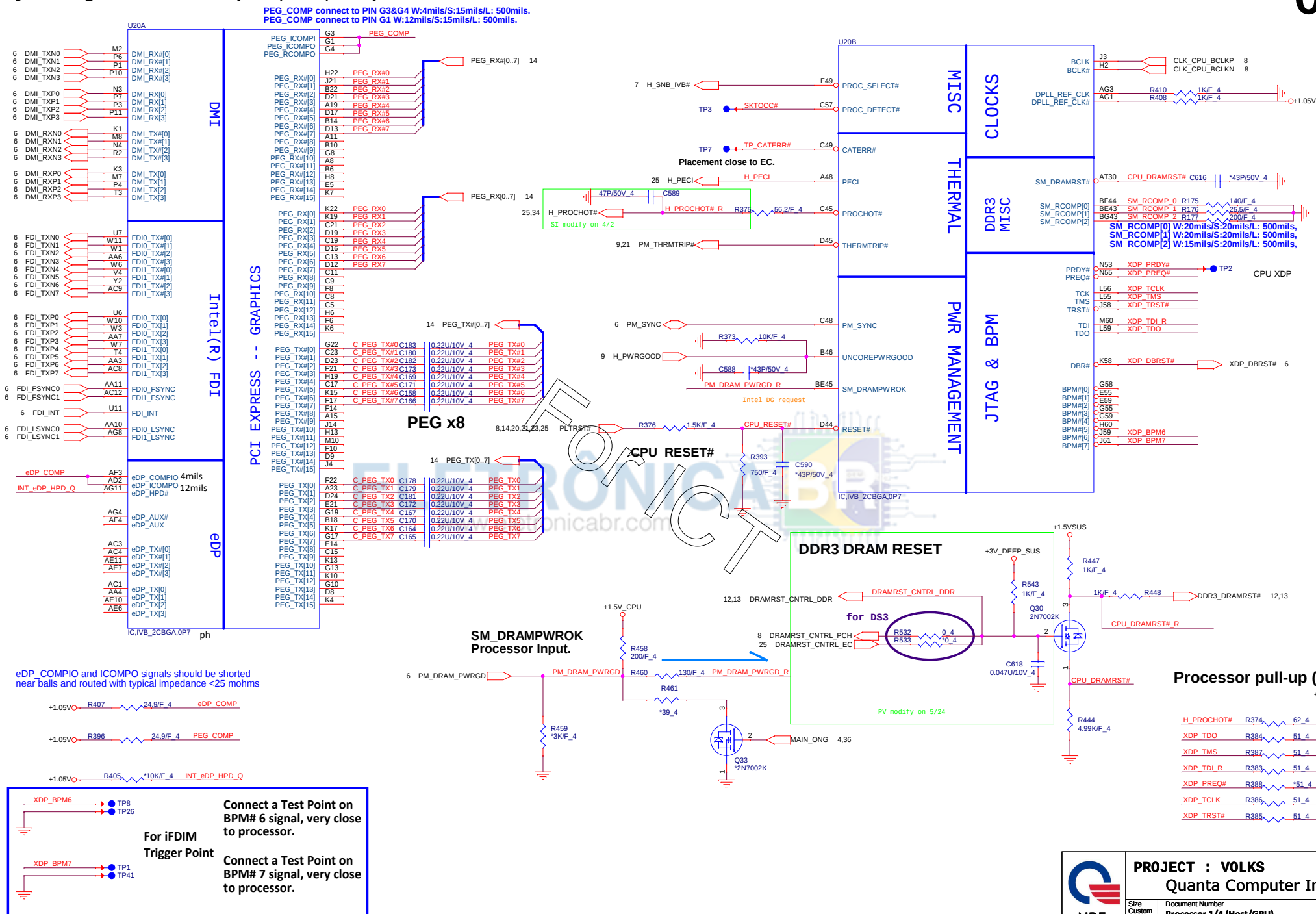
**NCP6132/NCP5911/RT8240P/
TP551462RGER**
Processor Power (+VCC_CORE/
+1.05_VTT/+VCCSA)

SLG55448V
System Discharge Power
(+1.5V/+3V/+5V)

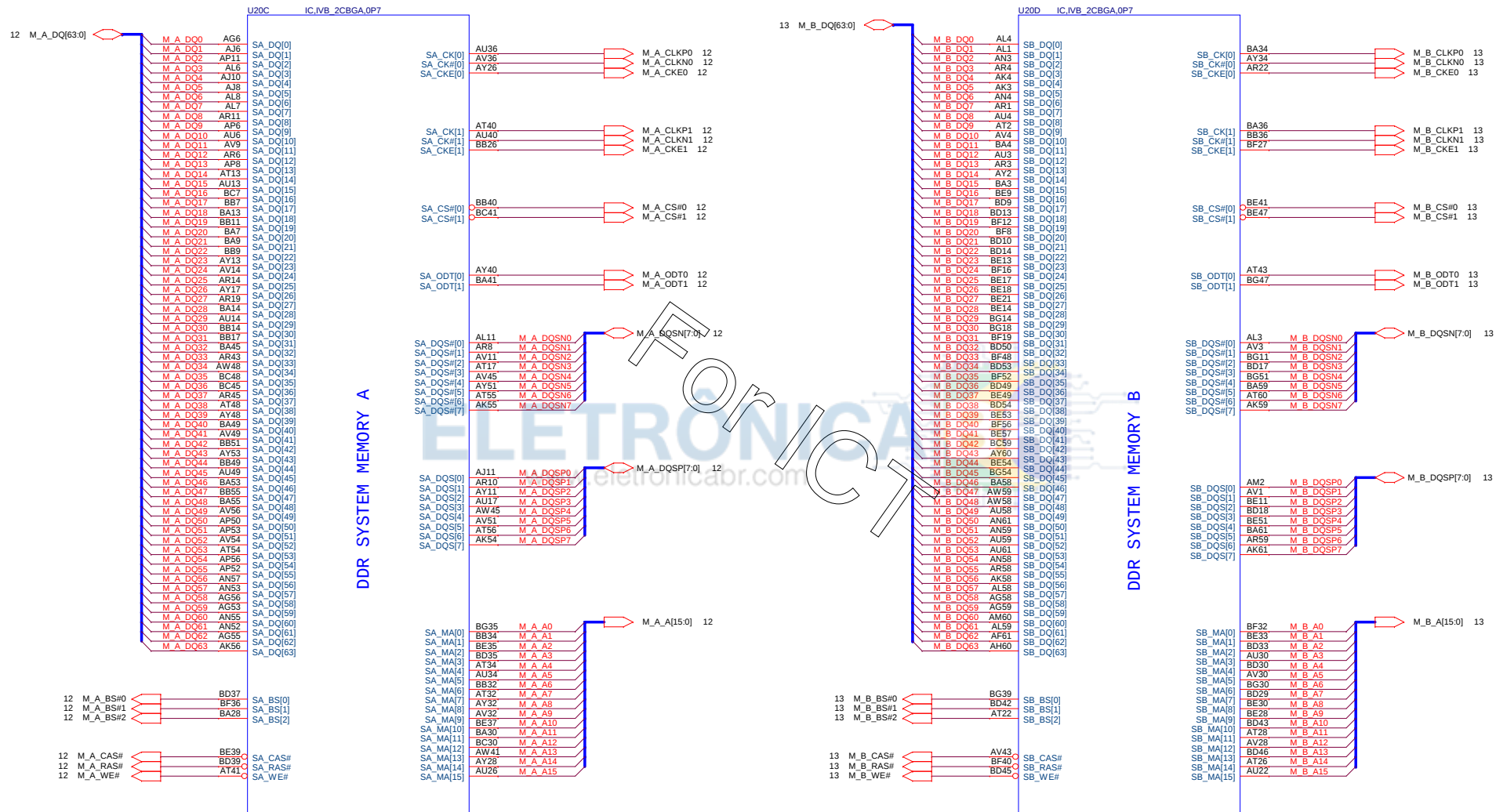
Richtek RT8207
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

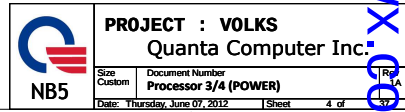
NCP3218G
GPU core power(+VGACORE)

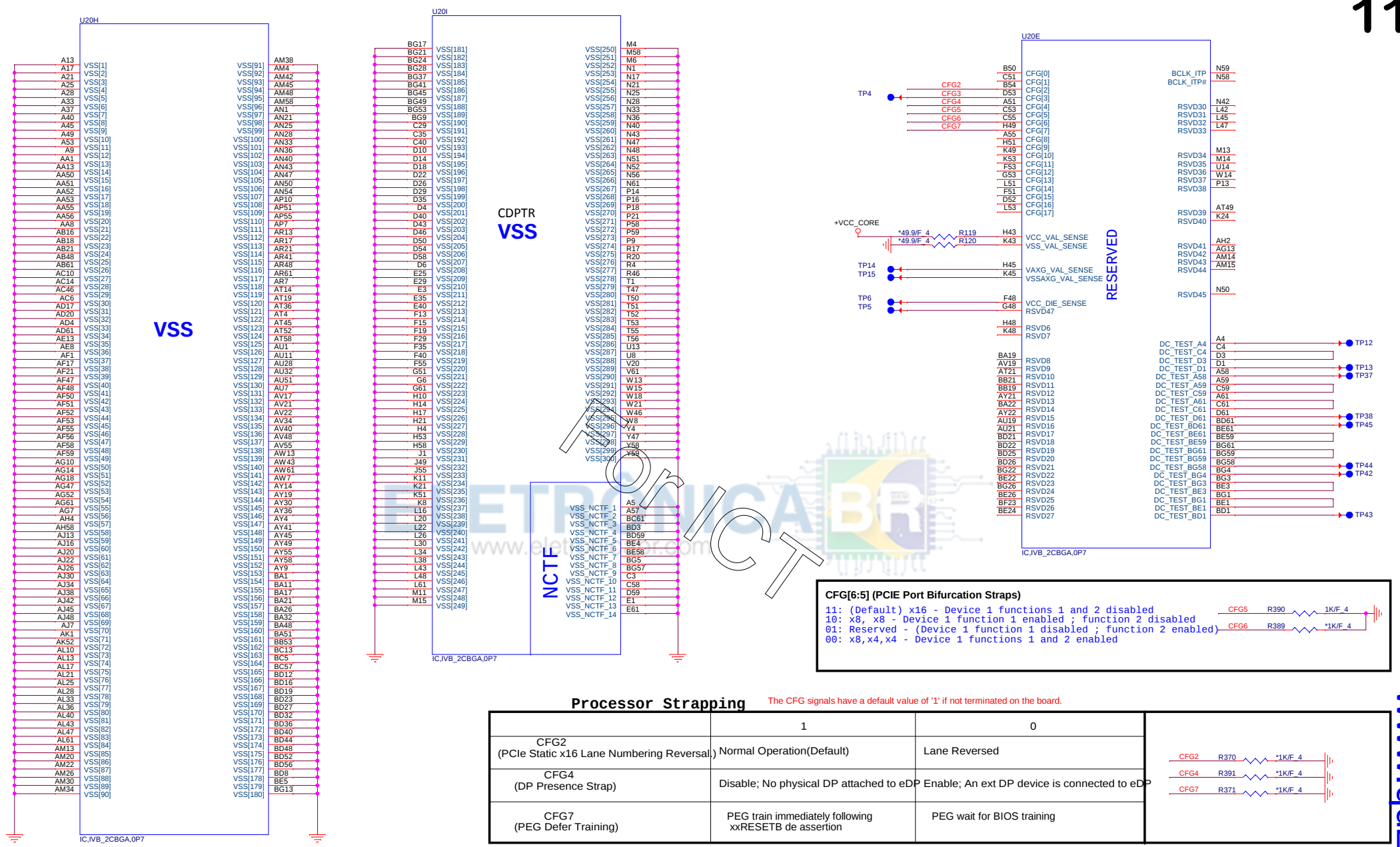
Ivy Bridge Processor (DMI, PEG, FDI)

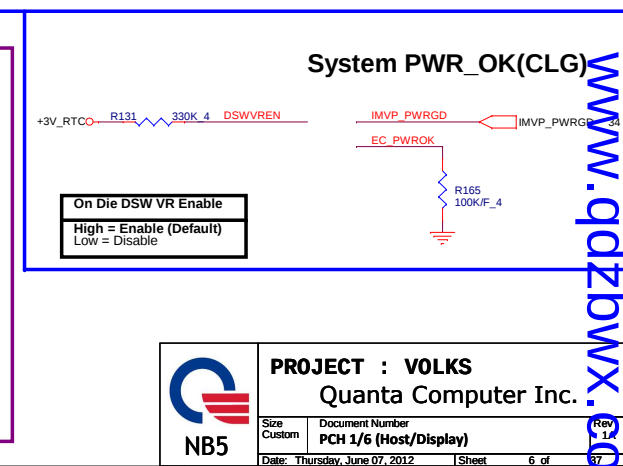
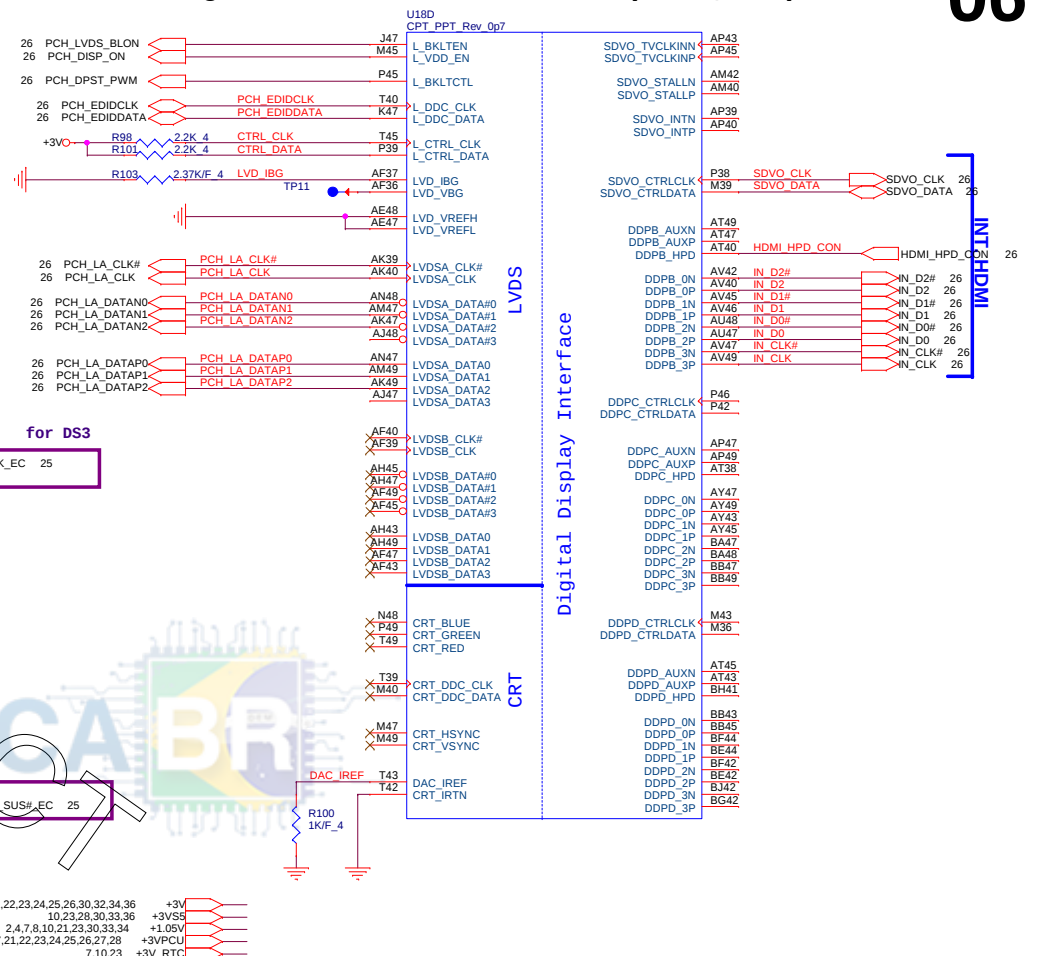


Ivy Bridge Processor (DDR3)

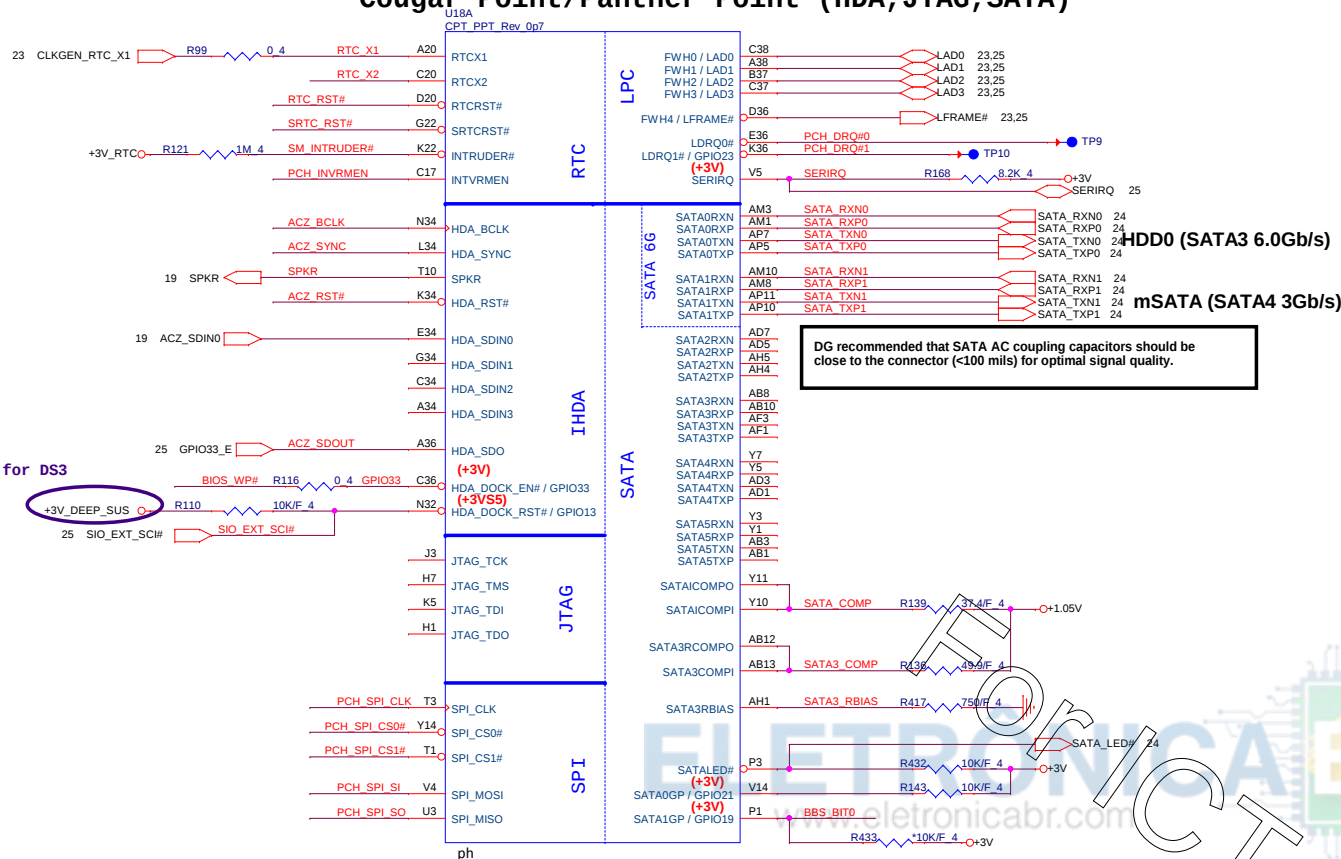








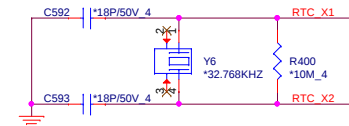
Cougar Point/Panther Point (HDA, JTAG, SATA)



PCH Strap Table

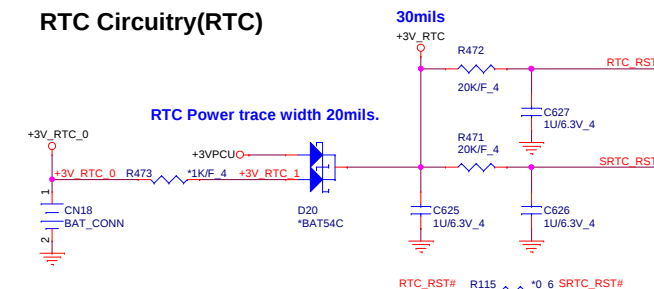
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V ₀ R152 1K/F 4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R363 1K/F 4 R364 10K/F 4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V _{RTC0} R122 330K 4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R104 1K/F 4 ACZ_SDOOUT ACZ_SDOOUT 25
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R419 1K/F 4 BBS_BIT0 8
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R354 1K/F 4 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V ₀ R416 1K/F 4 INV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V ₀ R415 2.2K 4 R414 1K/F 4 INV_CLE 9 H_SNB_IVB# 2
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.8V	for DS3 +3V _{DEEP_SUS} 0 R135 1K/F 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V _{DEEP_SUS} 0 R105 1K/F 4 ACZ_SDOOUT
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MISO	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

RTC Clock 32.768KHz

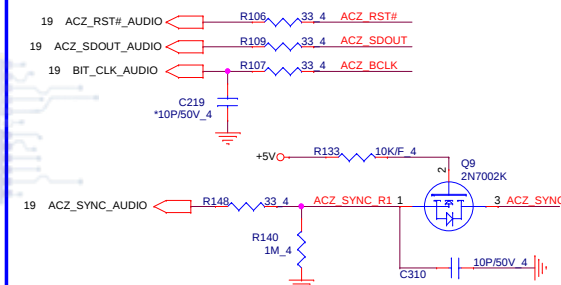


no stuff if use green Clock

RTC Circuitry(RTC)

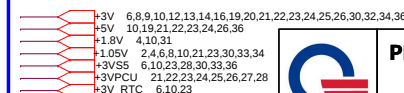
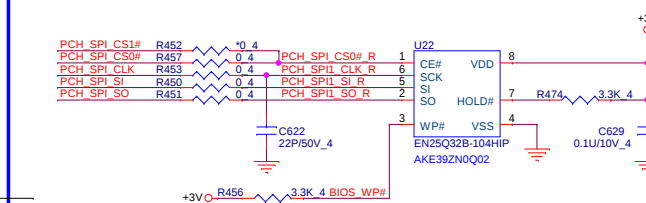


HDA Bus(CLG)



Vender	Size	P/N
EON	4MB	AKE392N0Q02 (EN25Q32B-104HIP)
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

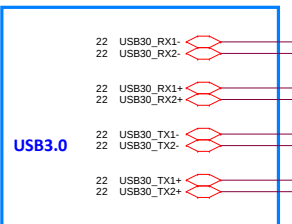
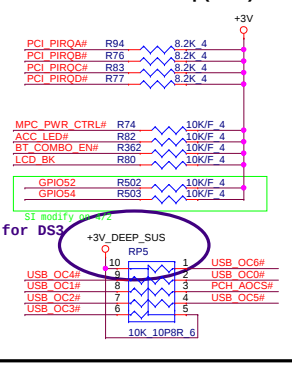
PCH SPI ROM(CLG)



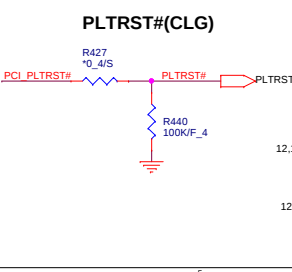
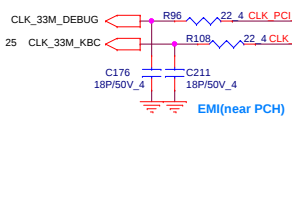
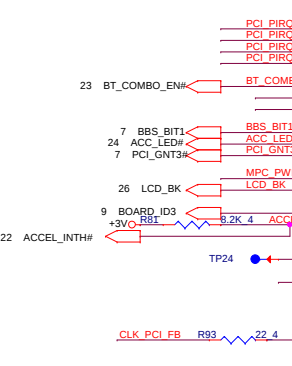
PROJECT : VOLKS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (HDA/RTC/SATA/SPI)	1.1
Date: Thursday, June 07, 2012	Sheet	7 of 67

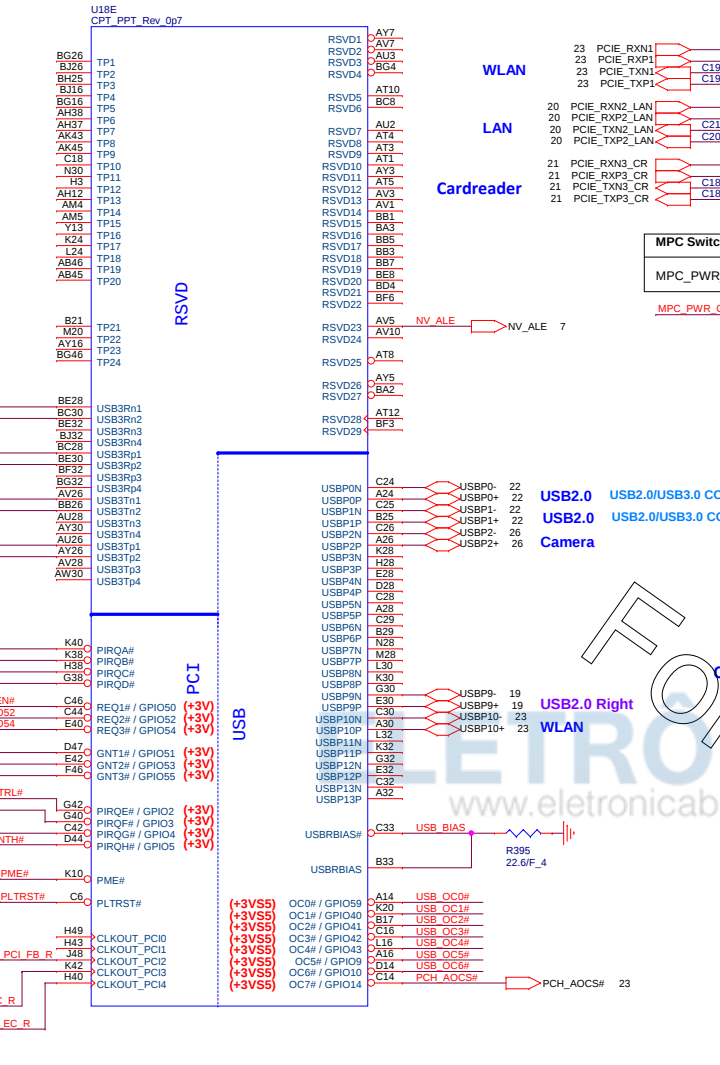
PCI/USBOC# Pull-up(CLG)



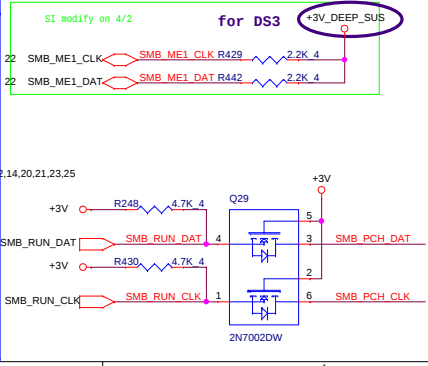
20111130 Modify USB3.0 for HM70



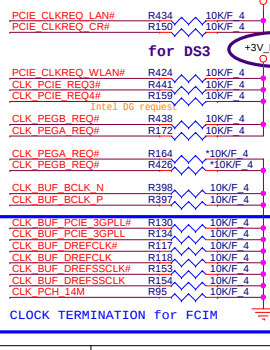
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



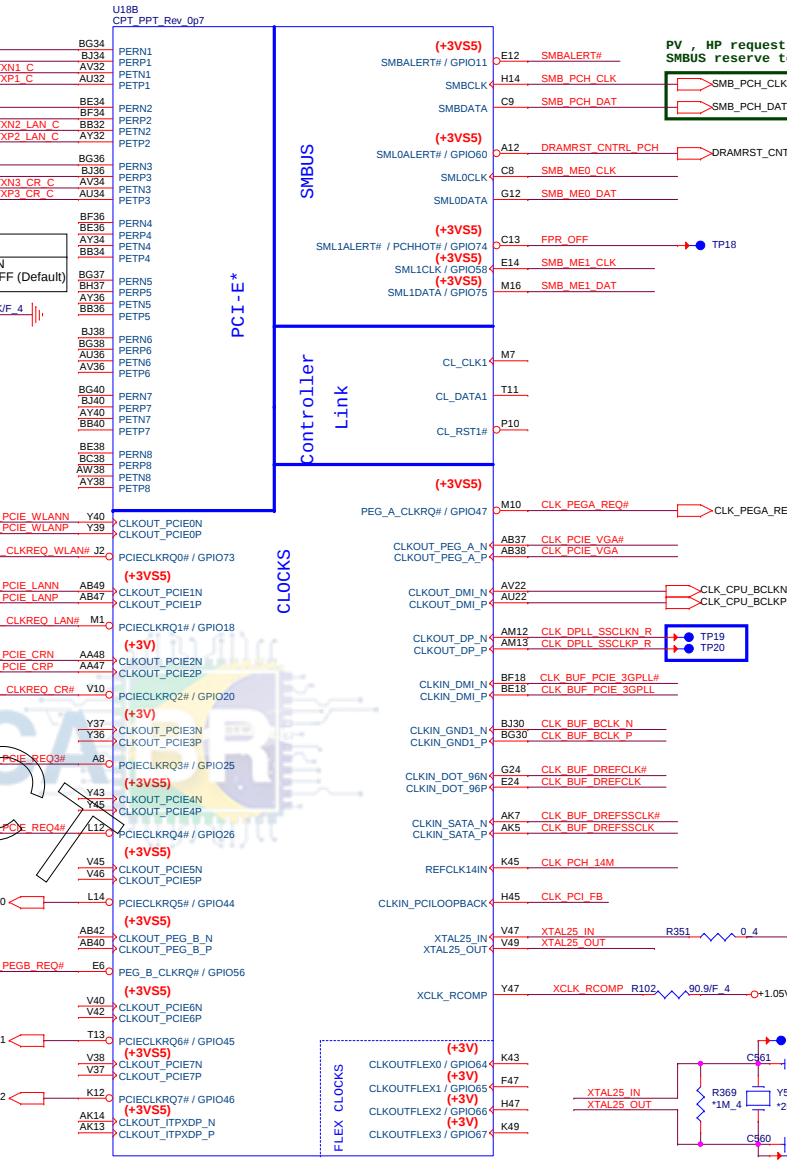
SMBus/Pull-up(CLG)



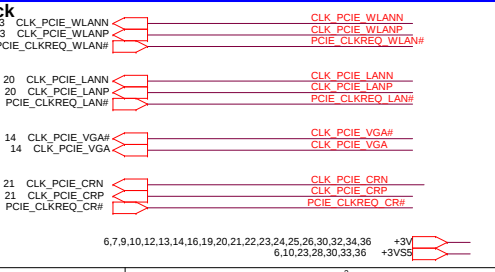
CLK REQ/Strap Pin(CLG)



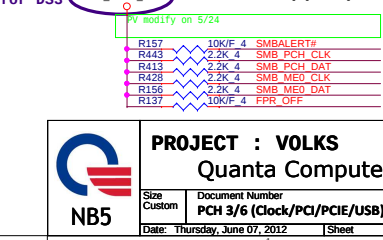
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



PCIE Clock

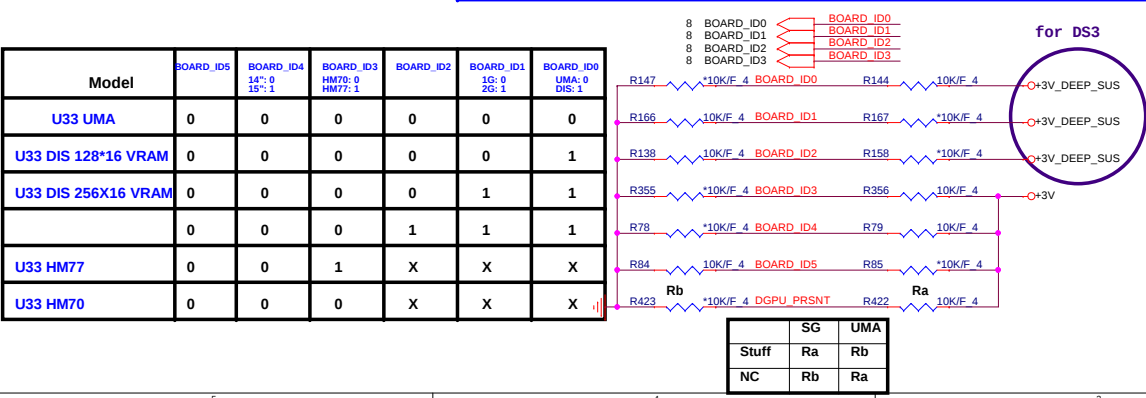


SMBus/Pull-up(CLG)



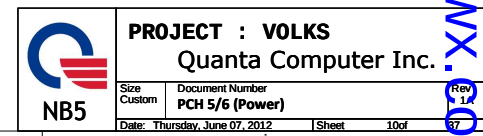
PROJECT : VOLKS
Quanta Computer Inc.
Size Custom Document Number
PCH 3/6 (Clock/PCI/PCIE/USB)
Date: Thursday, June 07, 2012 Sheet 8 of 37

OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36



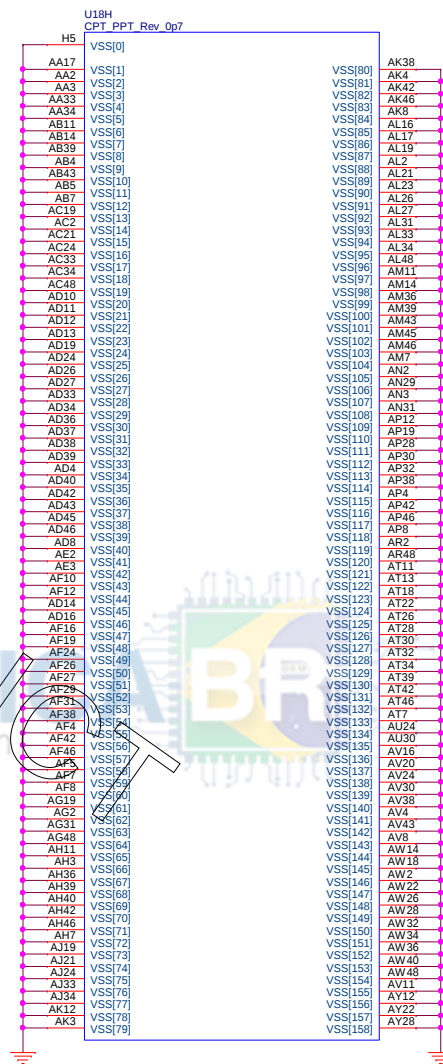
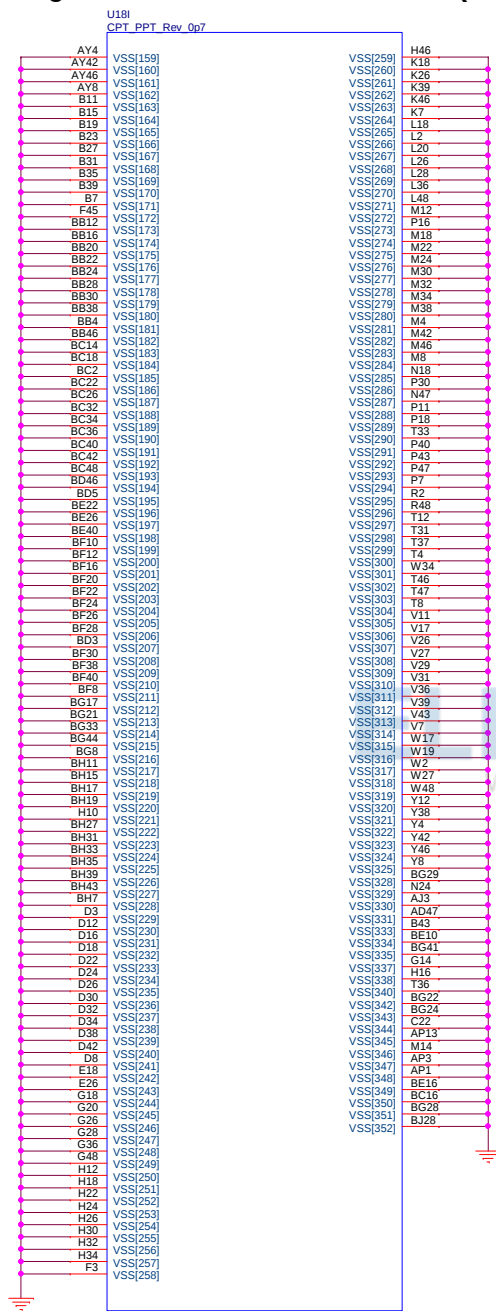
	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

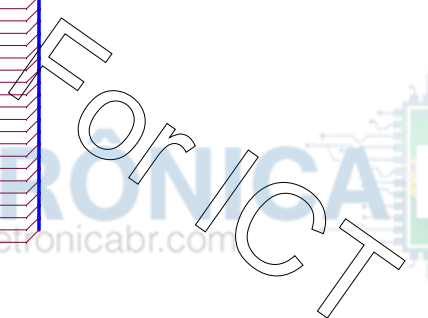
Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)





PC2100 DDR3 SDRAM SO-DIMM (204P)

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=4.0_STD
ddr-ddrsk-20401-tp4b-204p-ldv
DGMK4000326
IC SOCKET DDR3 SODIMM(204P,H4.0,STD

6,7,8,9,10,13,14,16,19,20,21,22,23,24,25,26,30,32,34,36 +3V

2,4,13,31,33 +1.5VSUS

13,31,36 +0.75V DDR VTT

SI modify on 4/25

U36 SI modify on 5/28

SI modify on 4/25

Diagram illustrating the 15V5VUS supply rail configuration. The rail is connected to a +15V5VUS source. The rail branches out to various components, each connected to a 10U/6.3V 4 or 10U/6.3VS 6 supply rail.

Component	Supply Rail
C349	10U/6.3V 4
C404	10U/6.3V 4
C411	10U/6.3V 4
C353	10U/6.3V 4
C402	10U/6.3VS 6
C397	10U/6.3VS 6
C351	10U/6.3VS 6
C354	10U/6.3VS 6
C407	10U/6.3VS 6
C394	10U/6.3VS 6
C350	10U/6.3V 6
C421	10U/6.3V 6
C440	10U/6.3V 6

+0.75V_DDR_VT

+SMDDR VREF DIMI

+SMDDR VREF DQ0

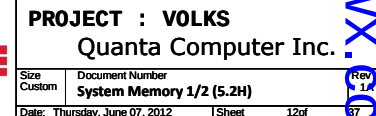
+3V

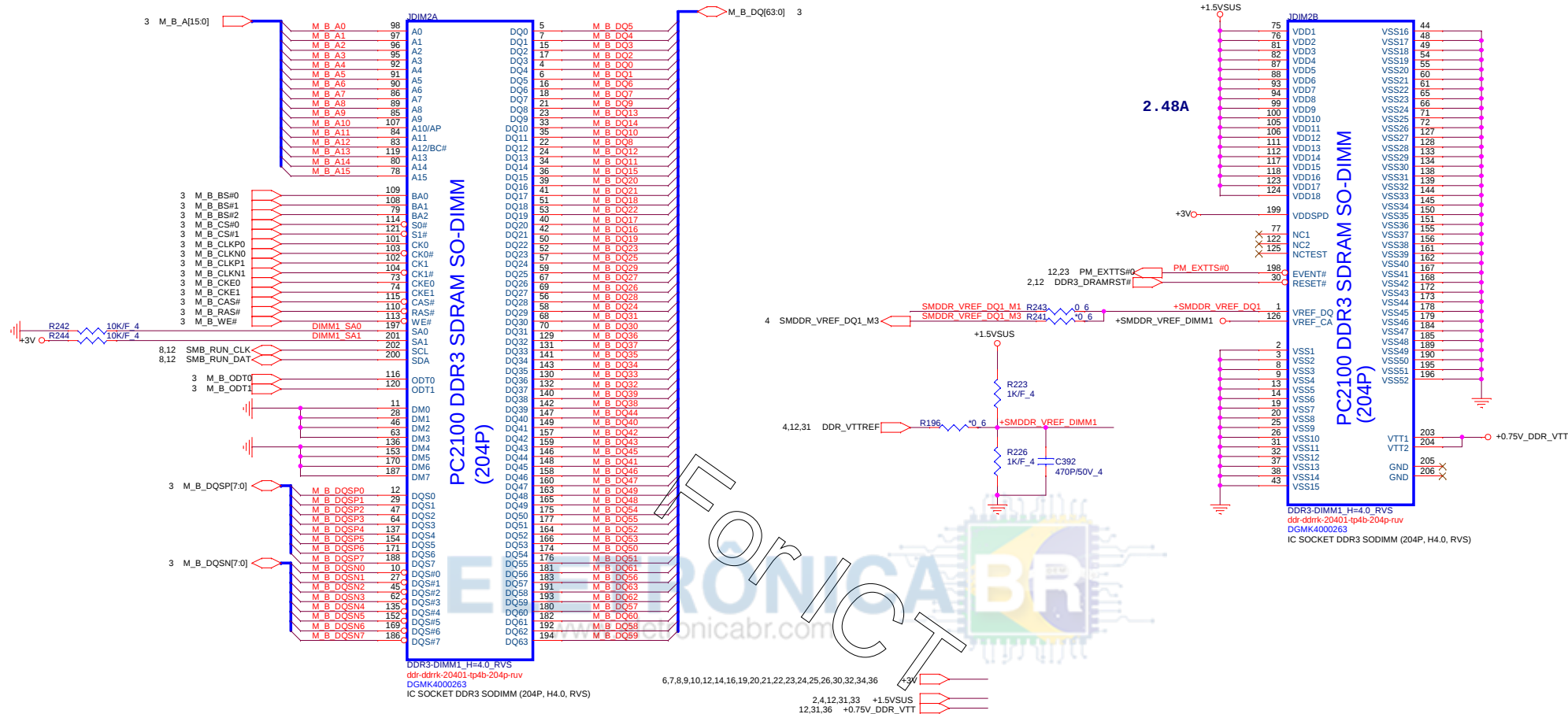
modify on 5/24

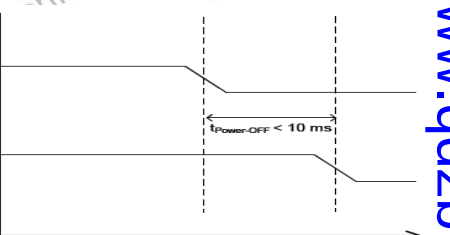
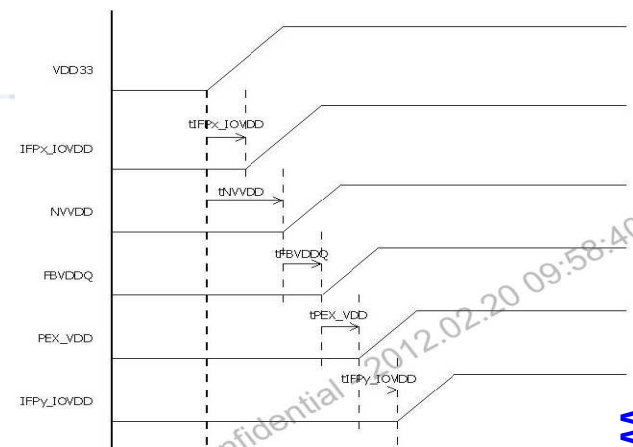
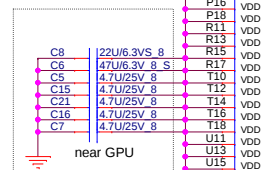
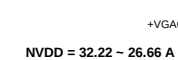
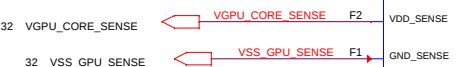
3 DRAMRST_CNTRL_DDR

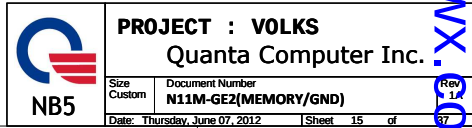
41331 DDR VTTB

REF R194

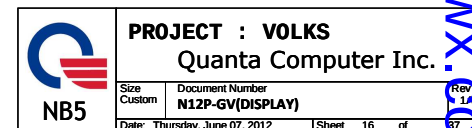


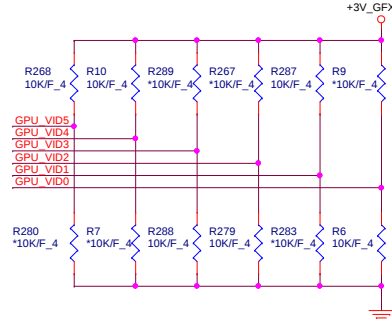




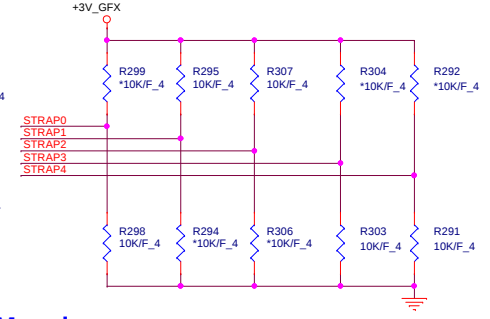
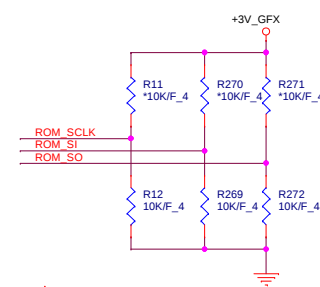
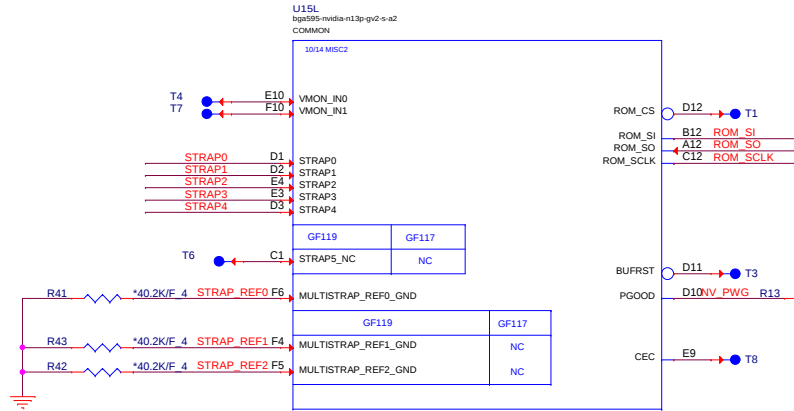


U15G





N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 0110010



Binary Strap Mode Mapping

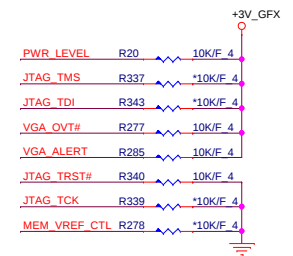
Strap Pin name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND (no dispaly)
STRAP0	RAMCFG[0]	10Kohm	USER defined
STRAP1	RAMCFG[1]	10Kohm	USER defined
STRAP2	RAMCFG[2]	10Kohm	USER defined
STRAP3	RAMCFG[3]	10Kohm	USER defined
STRAP4	PCIE_MAX_SPEED	10Kohm	Pull-down to GND

VRAM Configuration Table

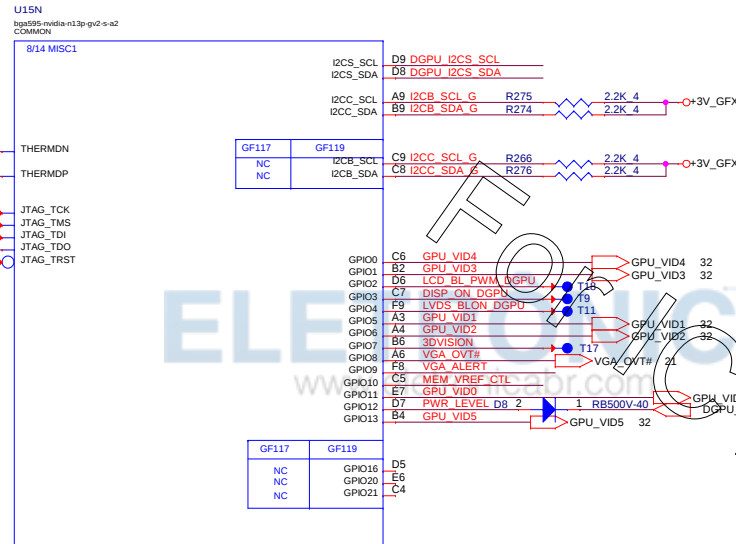
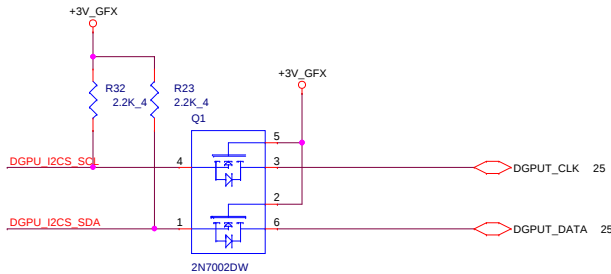
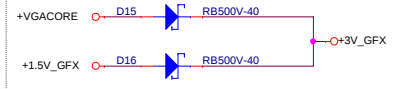
RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QBCON P/N	HP P/N
0011	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Reserved			
0101	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Hynix	H5TQ4G63MFR-11C	AKD5PGWTW00	AKD5PGWTW01
1100	DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Micron	MT41K256M16HA-107G:E	AKD5P6STL01	AKD5P6STL02
1011	DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Hynix	H5TQ2G63DFR-11C	AKD5MGWTW12	AKD5MGWTW13
		Samsung	K4W2G1646C-11C	AKD5MGWT513	AKD5MGWT508
0001	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Samsung	K4W4G1646B-11C	AKD5MGWT518	AKD5MGWT517
0100	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Hynix	H5TQ4G63AFR-11C	AKD5MGWT519	AKD5MGWT520
1011	DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Samsung	K4W2G1646E-11C	AKD5MGWT521	AKD5MGWT522

GB2-64 and GB4-128 GPIO Description

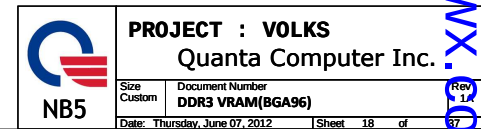
GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPU_VID4	O	GPU Core VDD VID4	Strap to boot NVDD
GPIO1	GPU_VID3	O	GPU Core VDD VID3	Strap to boot NVDD
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding	LCD_VCC: 100K pull-down PSI: 10K pull-up or pull-down; stuff as needed to disable phase shedding by default
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID1	O	GPU Core VDD VID1	Strap to boot NVDD
GPIO6	GPU_VID2	O	GPU Core VDD VID2	Strap to boot NVDD
GPIO7	3Dvision	O	3D Vision Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	GPU_VID0	O	GPU Core VDD VID0	Strap to boot NVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	O	GPU Core VDD VID5	Strap to boot NVDD
GPIO14	HPD_AB	I	Hot Plug Detect for IFPA	See Figure 76
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 76
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID	PSI: 10K pull-up or pull-down; stuff as needed to disable phase shedding by default MEM_VDD_CTL: Strap to boot FBVDD/Q
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 76
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 76
GPIO19	HPD_F	I	Hot Plug Detect for IFPF	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			

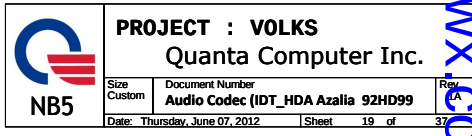


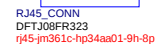
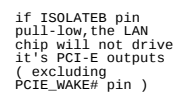
for meet Power down sequence.
Nvidia request for optimus



14.16.32.33 +3V_GFX

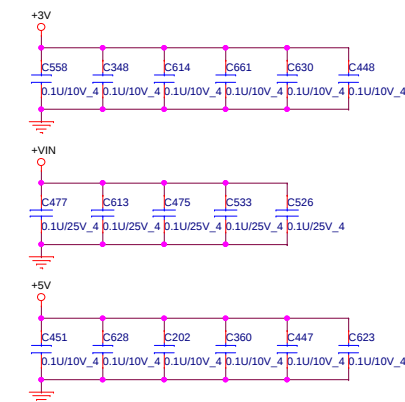
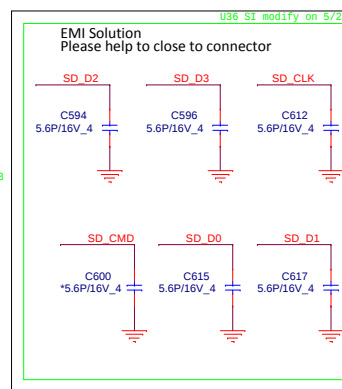
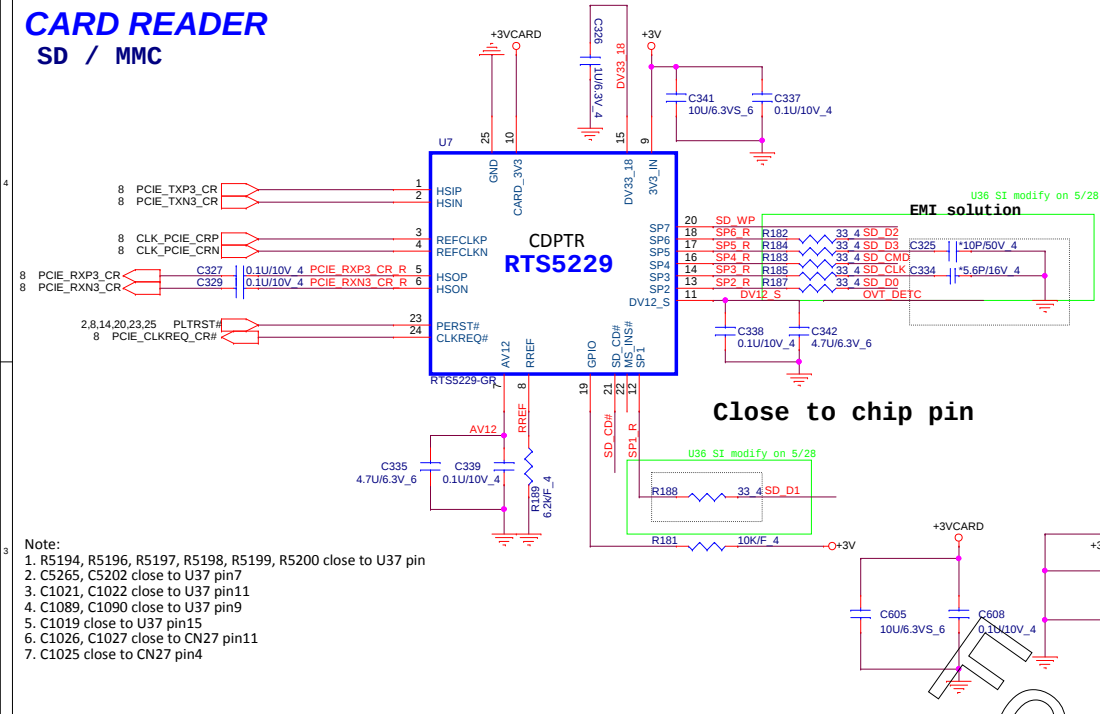




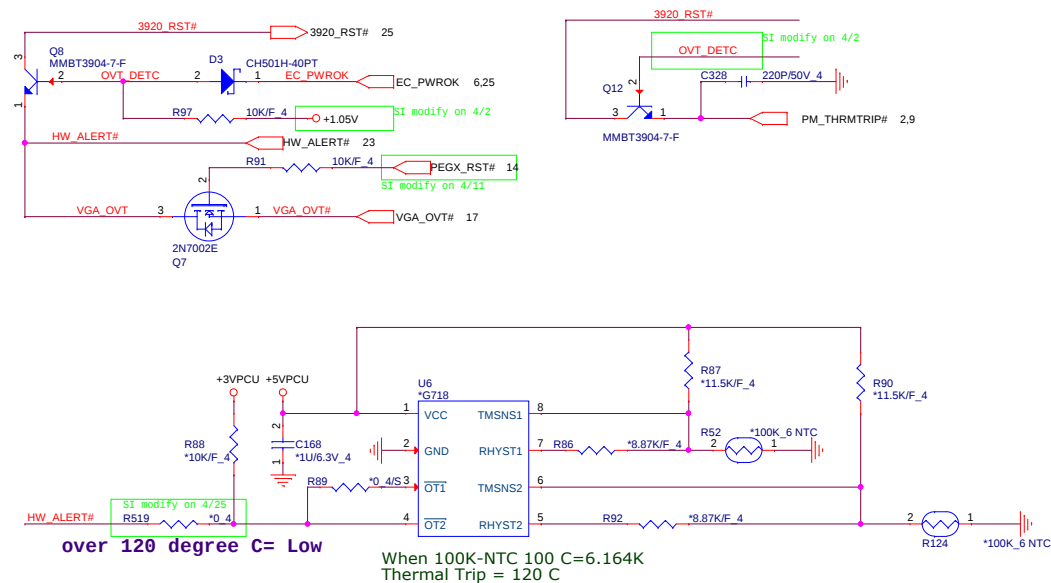


CARD READER

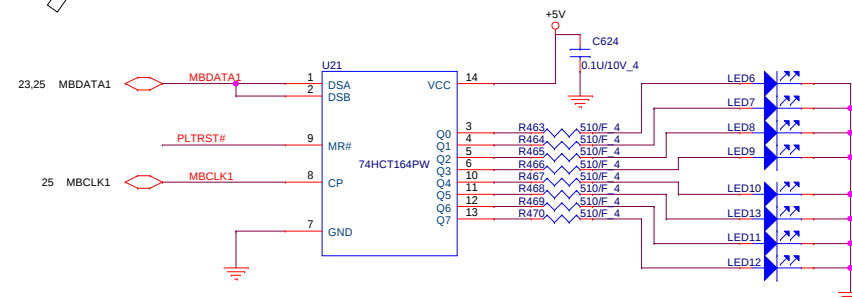
SD / MMC



Thermal HW protect

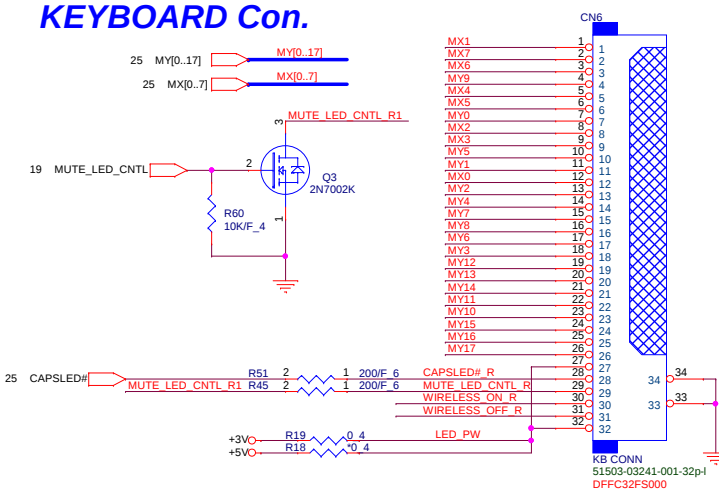


80 port

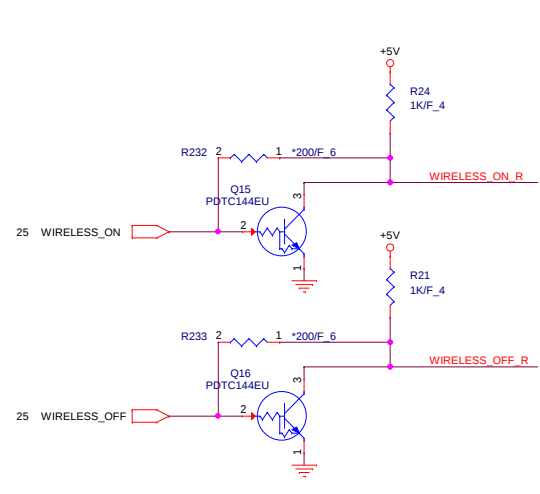
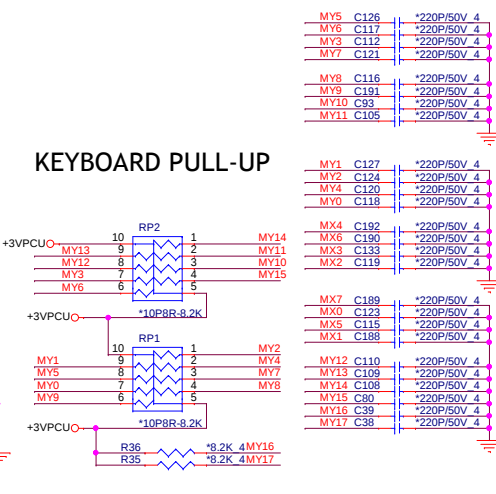


KEYBOARD Con.

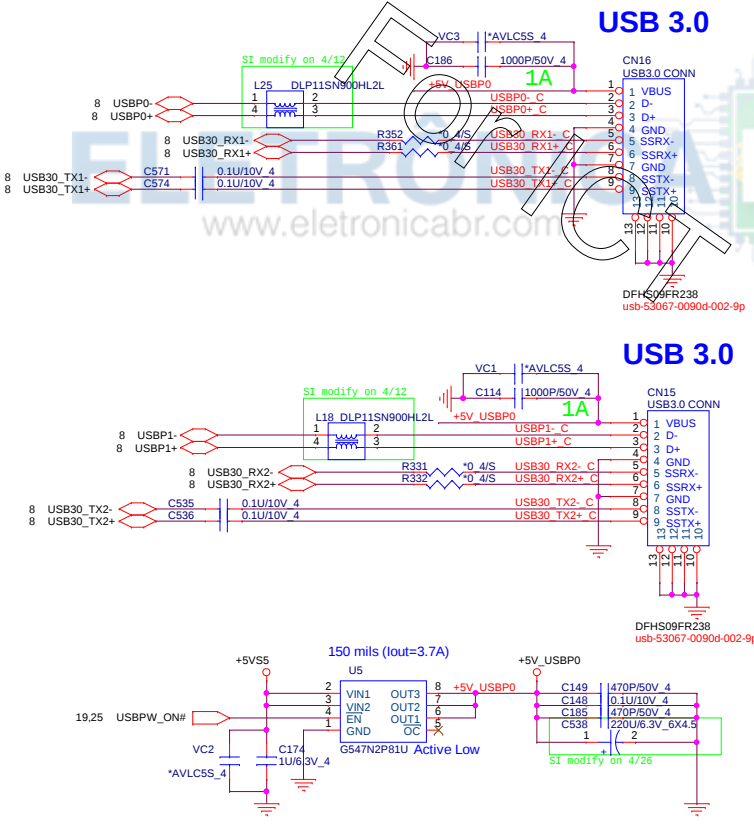
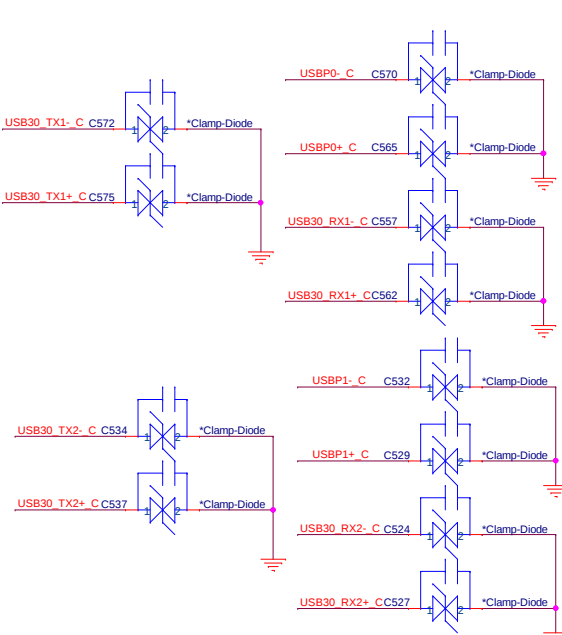
22



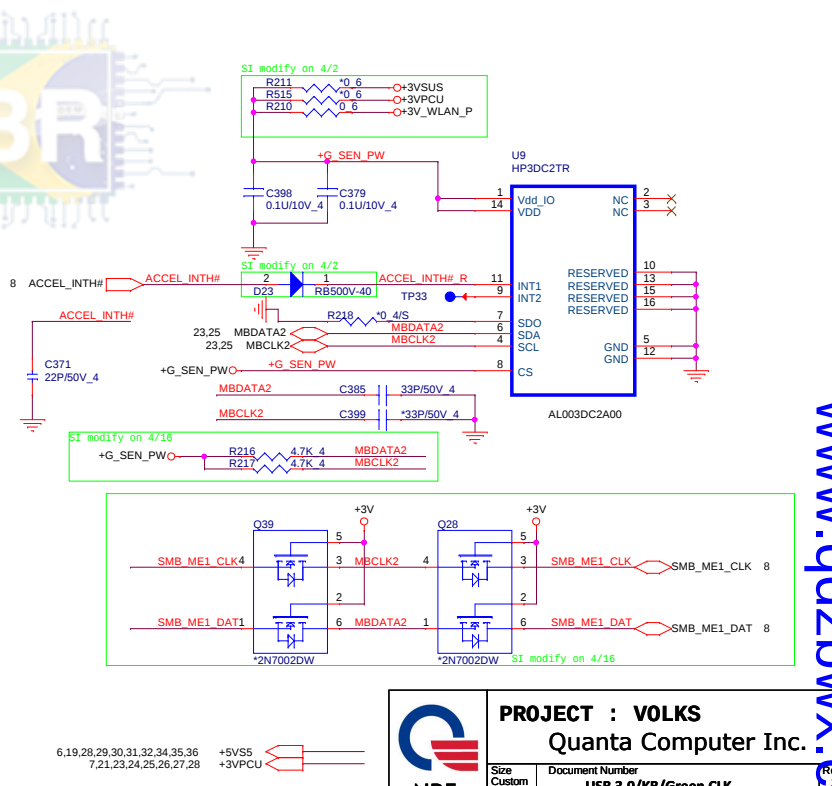
KEYBOARD PULL-UP



USB 2.0/3.0 Combo



Accelerometer Sensor



PROJECT : VOLKS
Quanta Computer Inc.

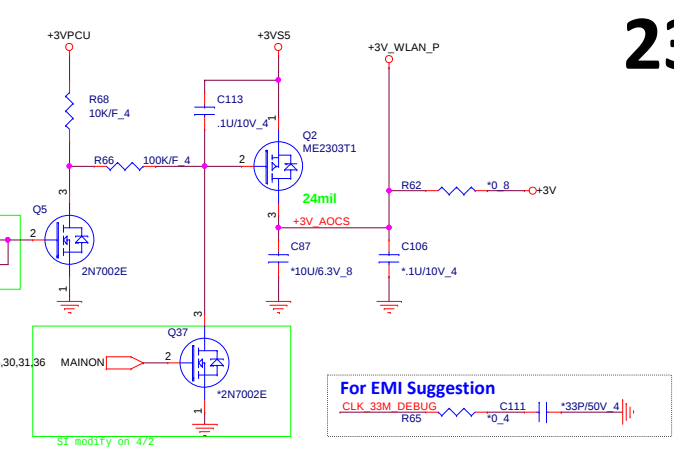
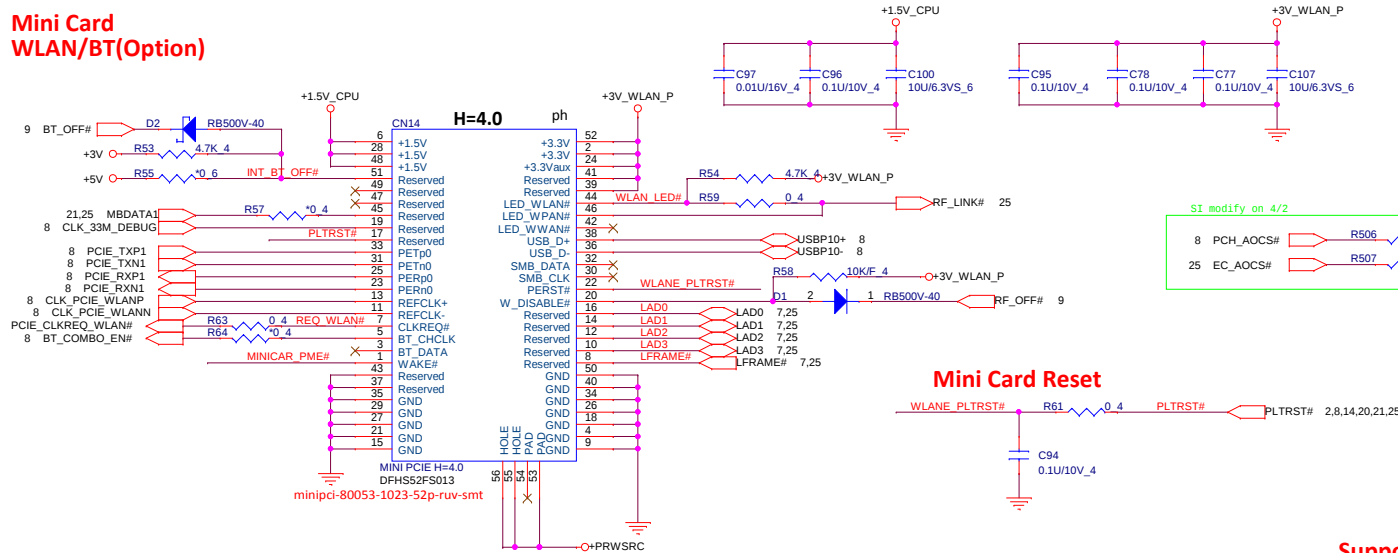
Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	1.1

Date: Thursday, June 07, 2012 | Sheet: 22 of 27

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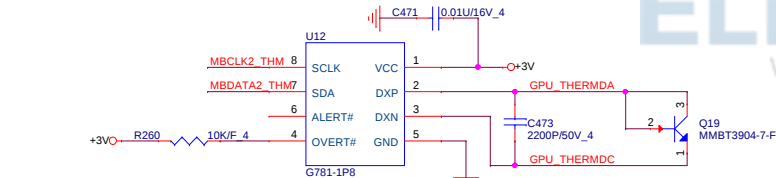
Mini Card WLAN/BT(Optional)

23

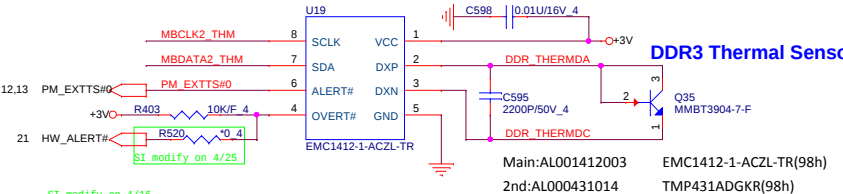


Local Thermal Sensor

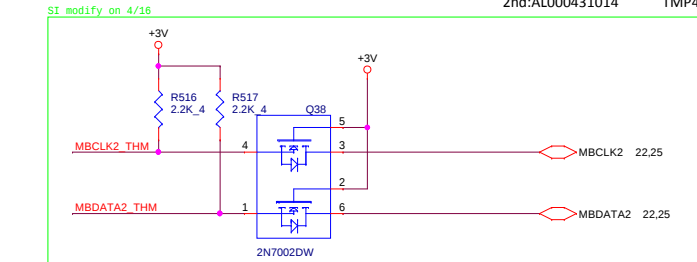
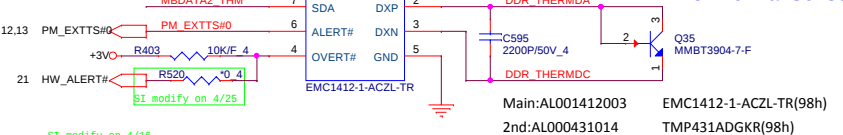
GPU Thermal Sensor



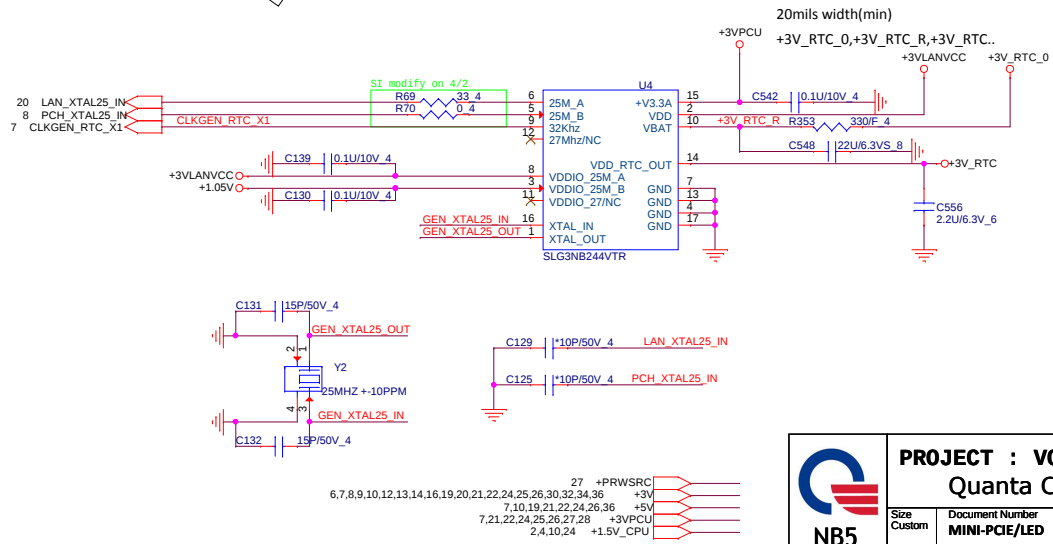
CPU Thermal Sensor



DDR3 Thermal Sensor

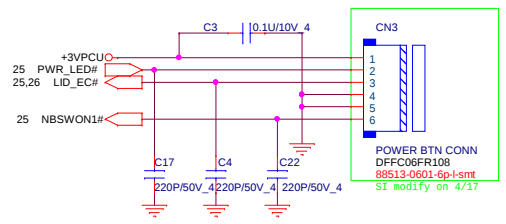


Green CLK Circuitry

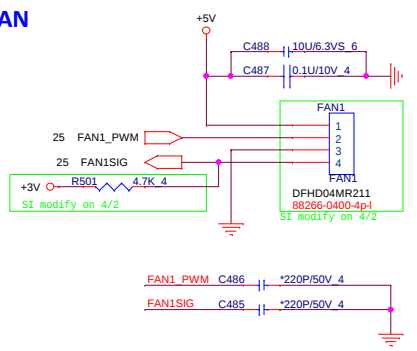


Power Button Connector

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



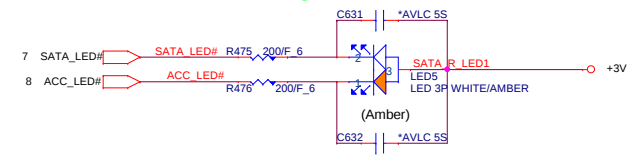
FAN



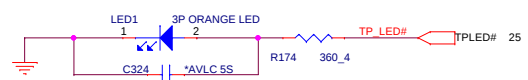
PWR LED



SATA LED

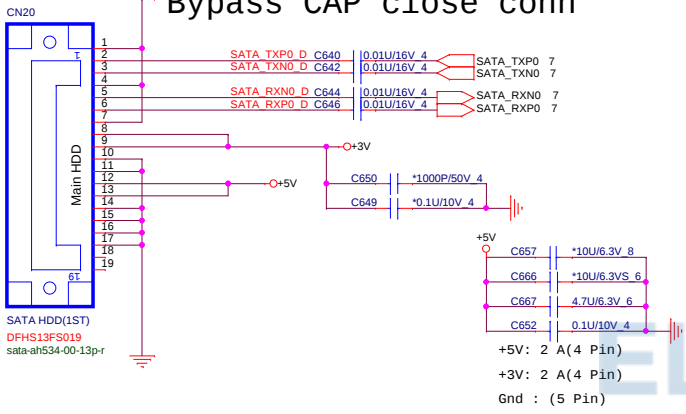


14" TP LED

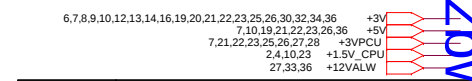
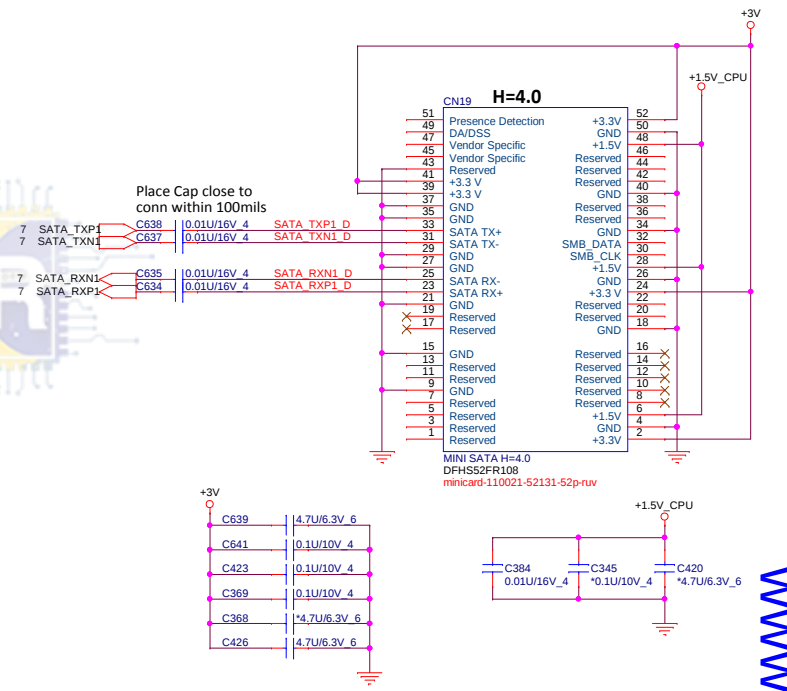


SATA HDD Connector(Cable type)

Bypass CAP close conn



Mini PCI-E Card 2- Full size mSATA



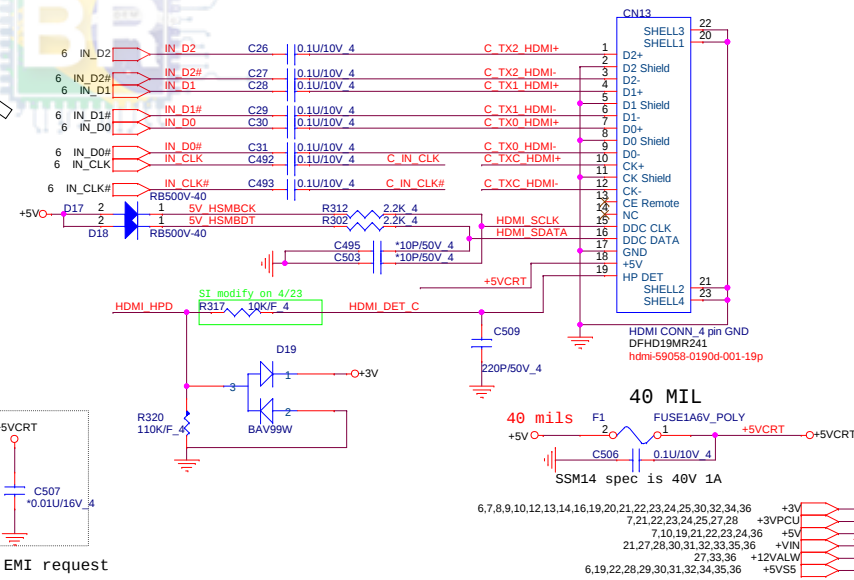
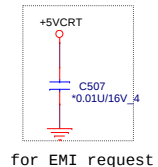
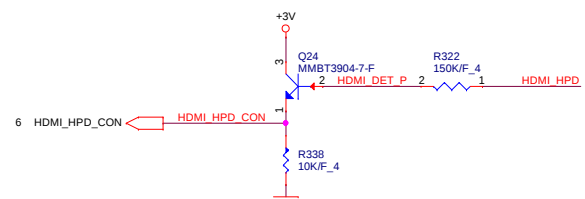
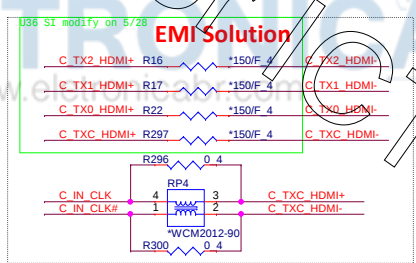
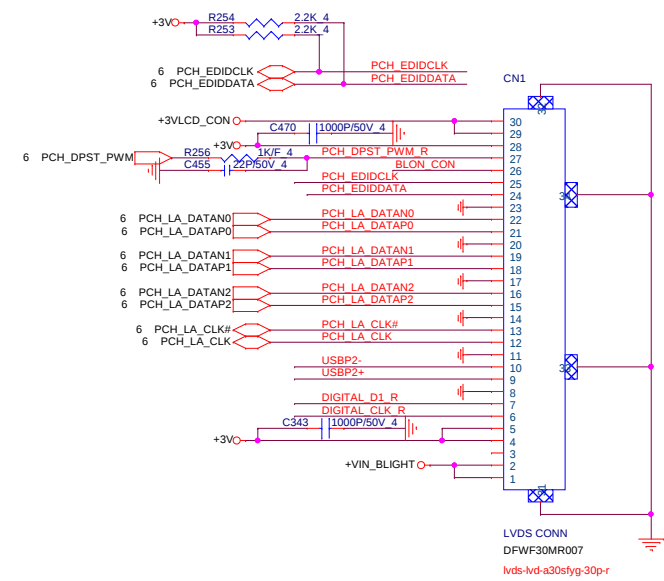
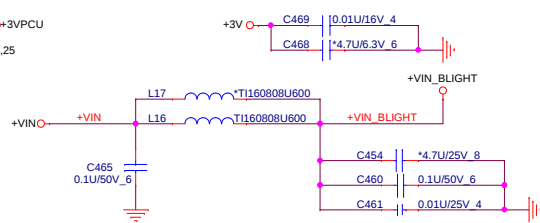
 NB5	PROJECT : VOLKS				
	Quanta Computer Inc.				
	Size	Document Number			Rev
	Custom	SATA HDD/ODD/MSATA CONN			1.1
Date: Thursday, June 07, 2012		Sheet	24of	37	

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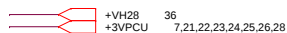


Size Custom	Document Number EC (KB3940 A1)/ROM	Rev 1.0
Date: Thursday, June 07, 2012	Sheet 25 of 27	

HDMI Conn.



 NB5	PROJECT : VOLKS Quanta Computer Inc..			 Rev 1.1
	Size Custom	Document Number LCD Connector (LVDS)		
Date: Thursday, June 07, 2012		Sheet	26of	37



+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

Current Limit setting
 $VILIMx = (RILIMx \times 10\mu A) / 10 = IILIMx \times RDS(ON)$
 $RILIMx = (IILIMx \times RDS(ON)) \times 10 / 10\mu A$

TONSEL= VREG5
Vout1=400kHz/Vout2=500kHz

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21,26,27,30,31,32,33,35,36
6,10,23,30,33,36
6,19,22,29,30,31,32,34,35,36
7,21,22,23,24,25,26,27

+VIN
+3VSS
+5VSS
+3VPCU

	PROJECT :VOLKS		
	Quanta Computer Inc.		
	Size Custom	Document Number 3/5VSS (RT8223P)	Rev A
	Date: Thursday, June 07, 2012	Sheet 28	of 37

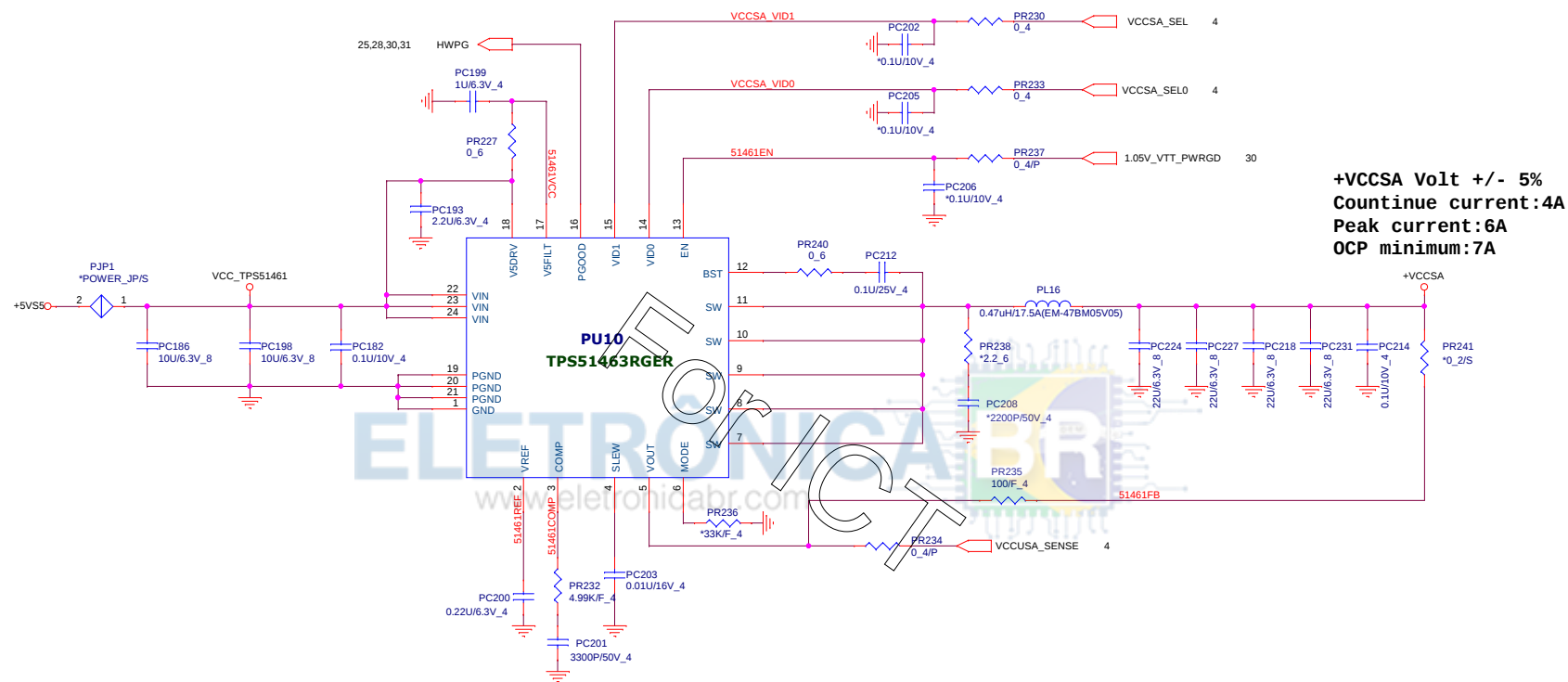
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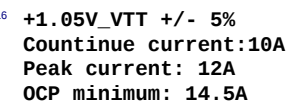
TPS51462RGER/AL051462000For CPU SV system agent
voltage slew rate of 0.5 -10 mV/ μ s

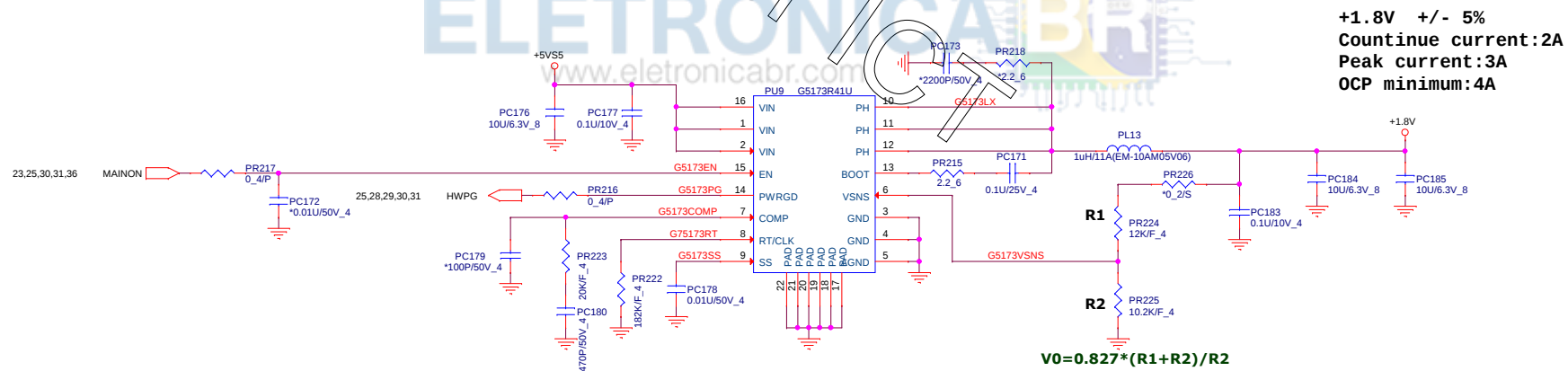
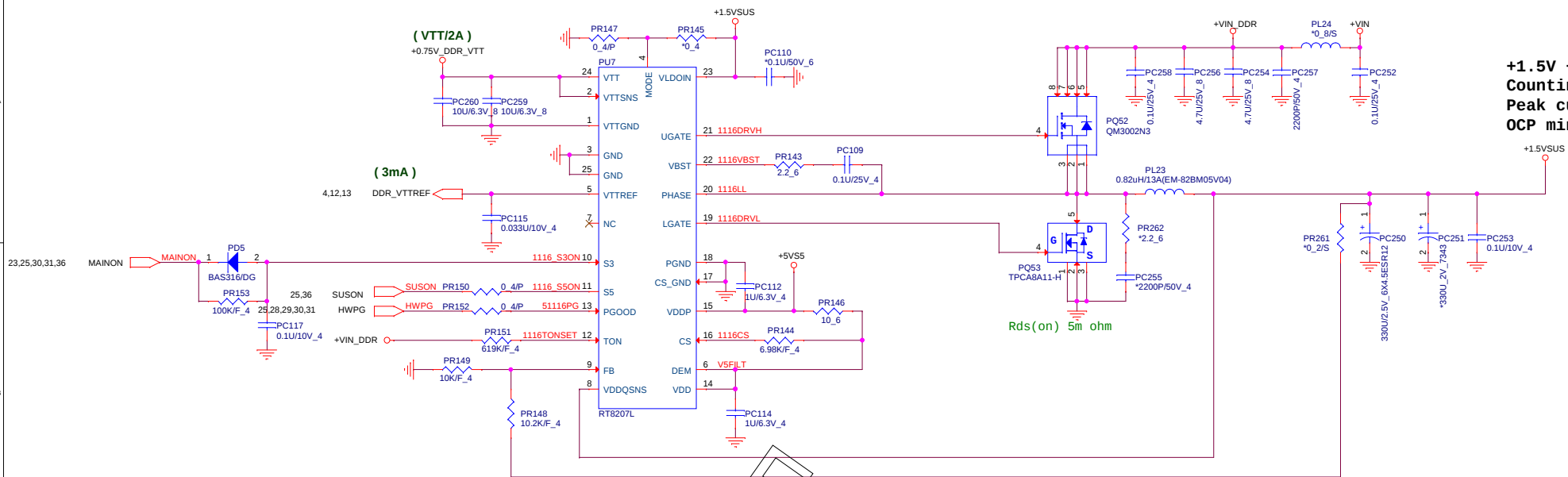
SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

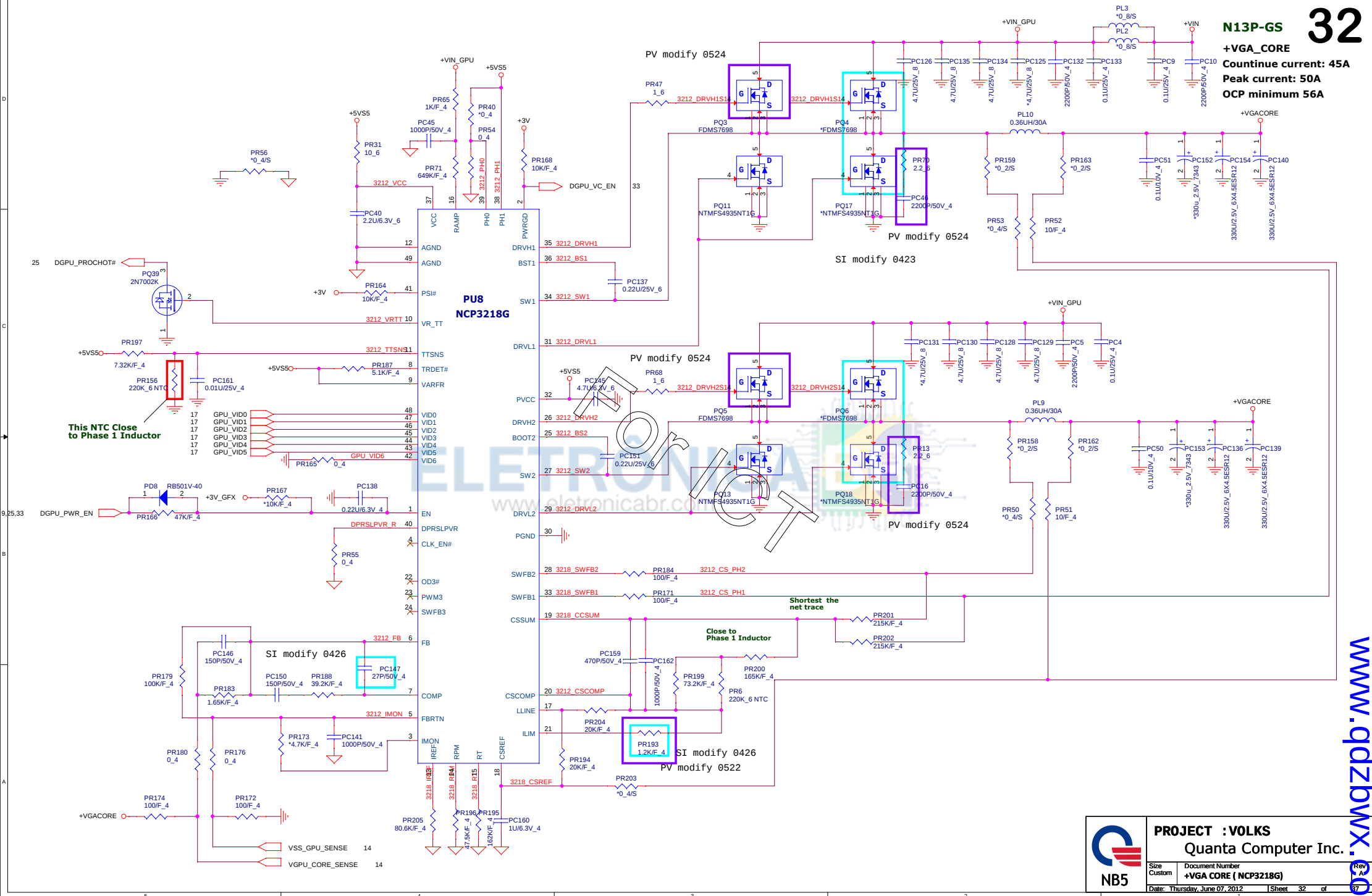
TPS51463RGER/AL051463000For CPU ULV system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V



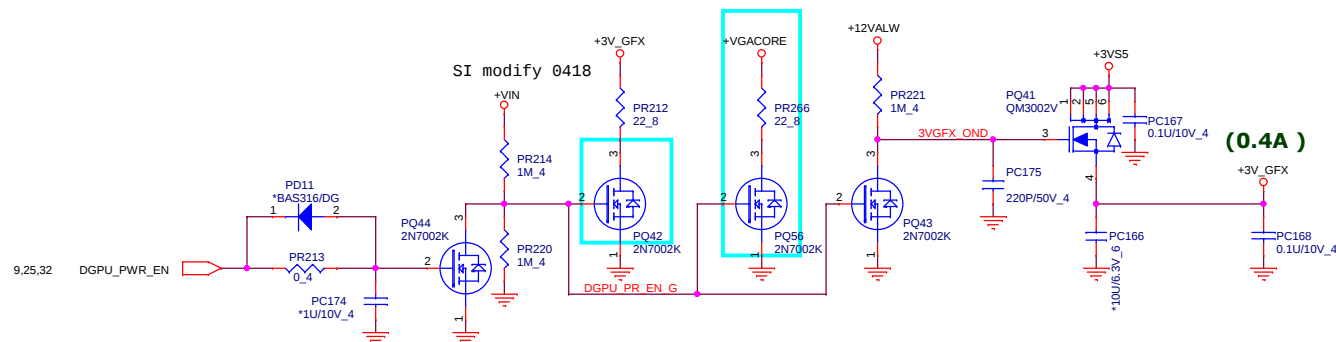




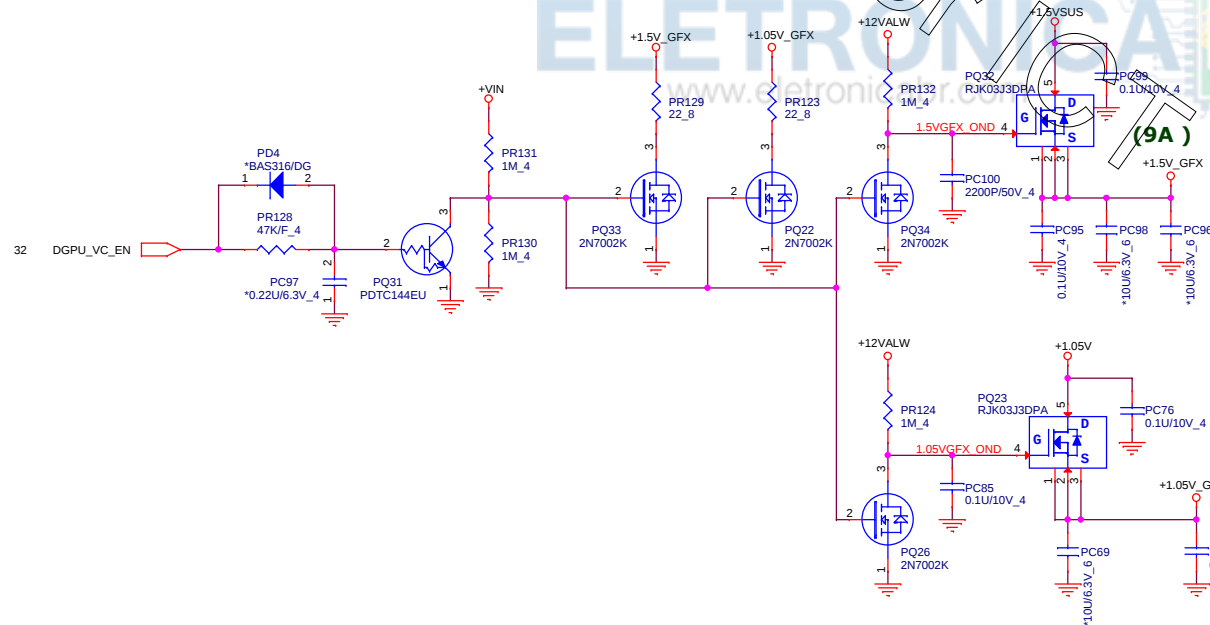


2,4,12,13,31 +1.5VSUS
 6,10,23,28,30,36 +3VSS
 14,16,17,32 +3V_GFX
 15,16,17,18 +1.5V_GFX
 14,15,16 +1.05V_GFX
 27,36 +12VALW
 2,4,6,7,8,10,21,23,30,34 +1.05V

SI modify 0418



(0.4A)



(9A)

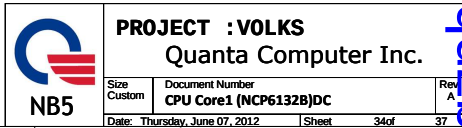
+1.05V +/- 3%
Continue current: 2.1A
Peak current: 3A



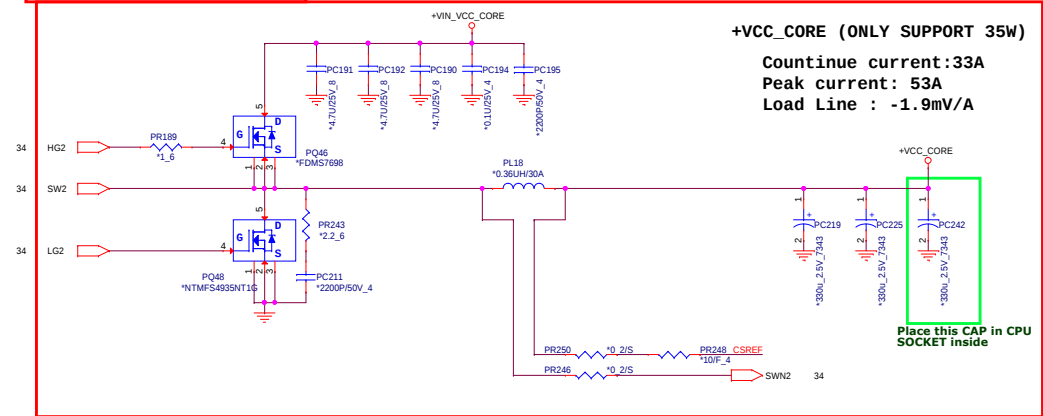
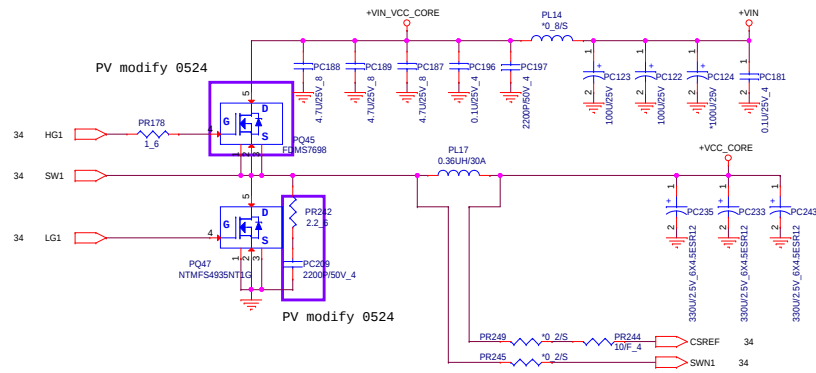
PROJECT :VOLKS
Quanta Computer Inc.

Size Custom Document Number **+VGA POWER** Rev A
 Date: Thursday, June 07, 2012 Sheet 33 of 37

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Dummy This Schematic
For CPU 1-Phase operation

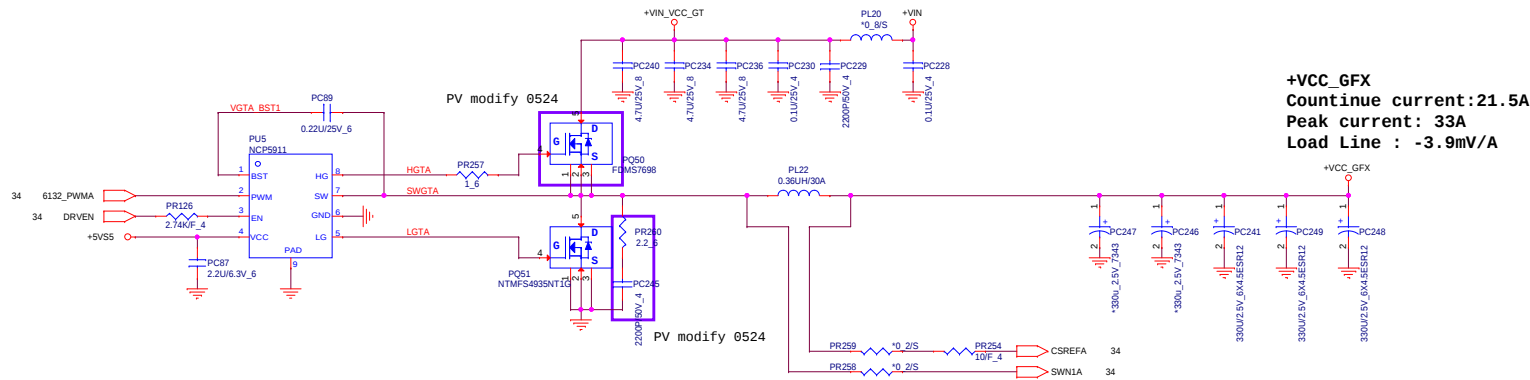


+VCC_CORE (ONLY SUPPORT 35W)

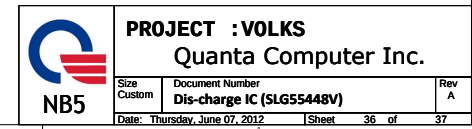
Countinue current:32A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ULV 17W)

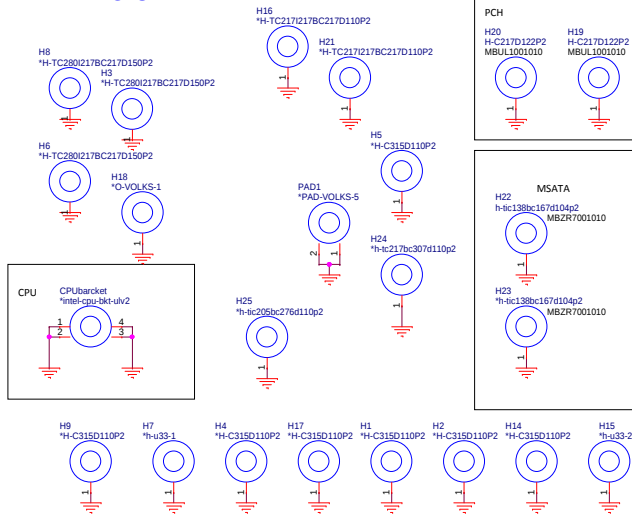
Countinue current:16A
Peak current: 33A
Load Line : -2.9mV/A



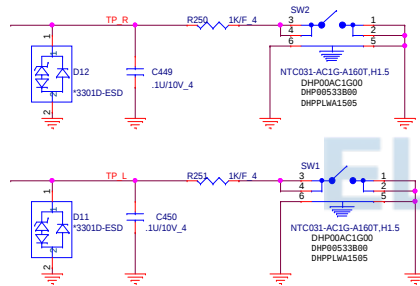
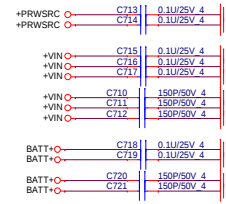
+VCC_GFX
Countinue current:21.5A
Peak current: 33A
Load Line : -3.9mV/A



14" Hole



EMI CAP for 14"



Touch Pad Connector

