

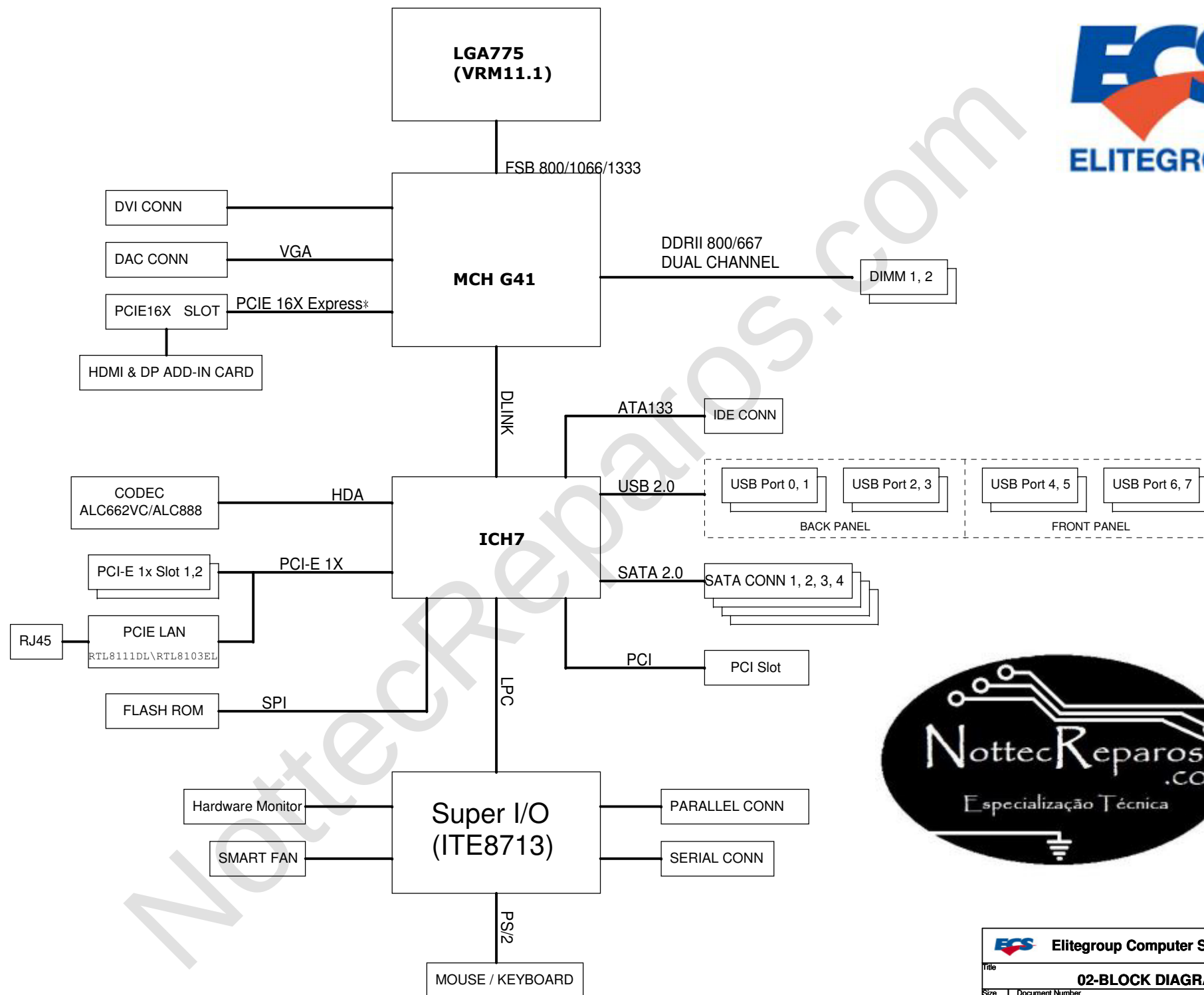
G41T-M7

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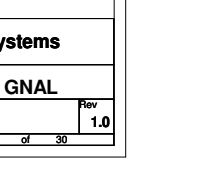
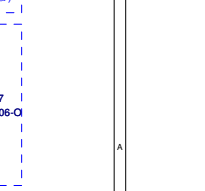
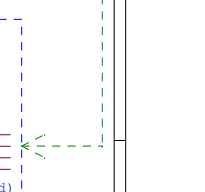
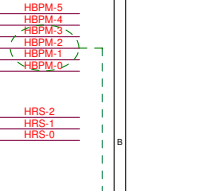
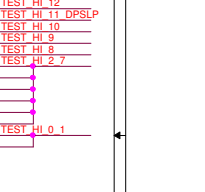
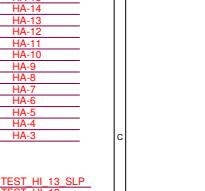
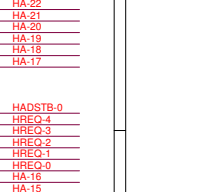
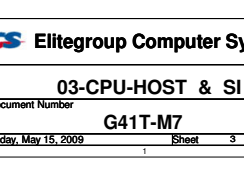
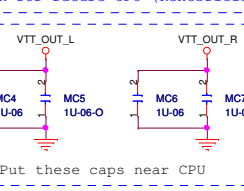
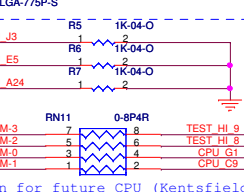
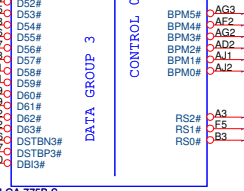
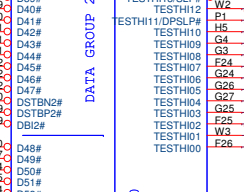
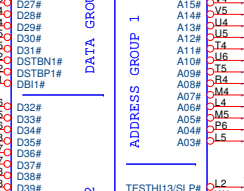
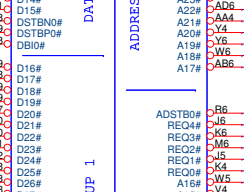
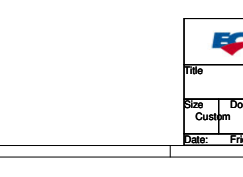
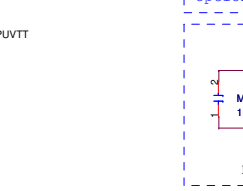
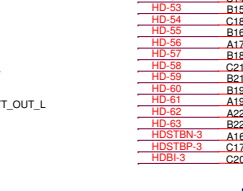
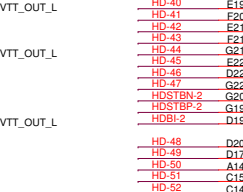
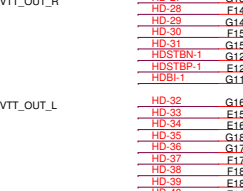
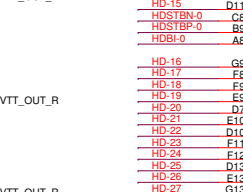
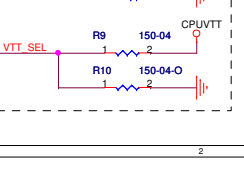
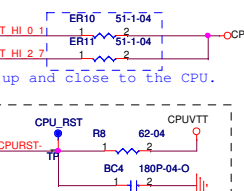
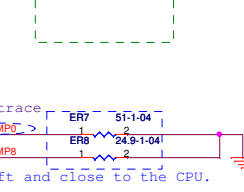
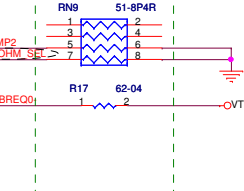
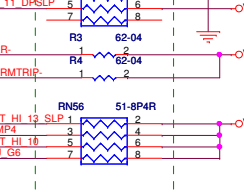
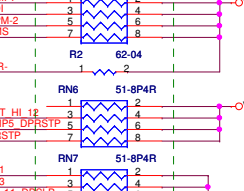
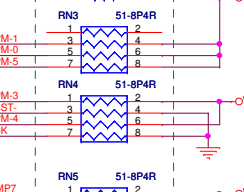
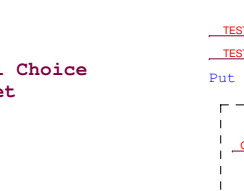
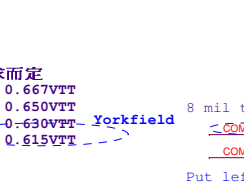
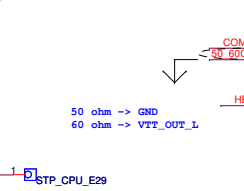
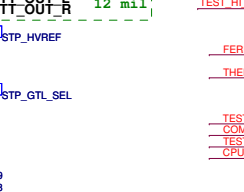
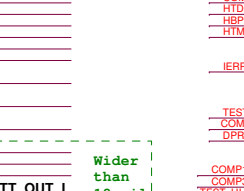
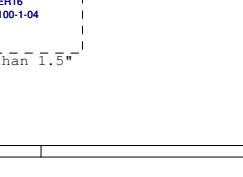
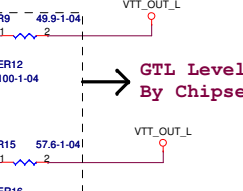
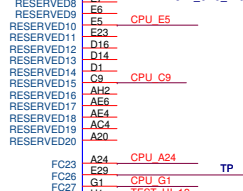
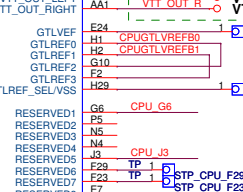
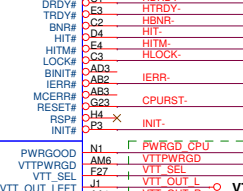
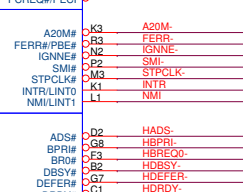
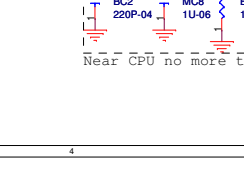
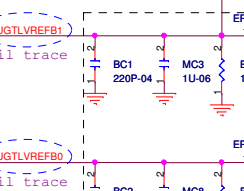
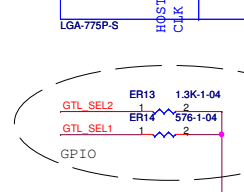
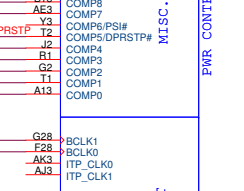
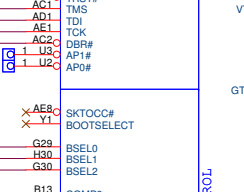
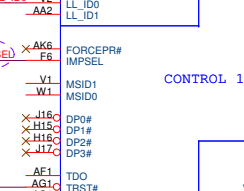
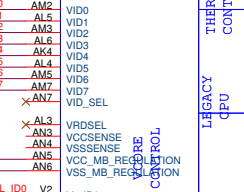
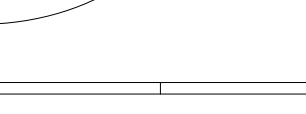
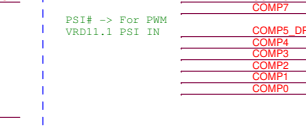
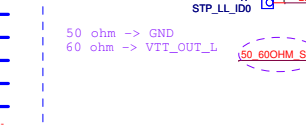
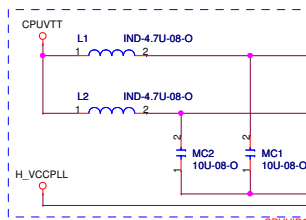


0 1	- C O V E R	P A G E
0 2	- B L O C K D I A G R A M	
0 3	- C P U - H O S T & S I G N A L	
0 4	- C P U - P W R & G N D	
0 5	- M C H - H O S T	
0 6	- M C H - D M I / P C I E / D A C / H D M I	
0 7	- M C H - M E M O R Y	
0 8	- M C H - P W R / G N D	
0 9	- I C H 7 - D M I / P C I E / S A T A / U S B / M I S C 1	
1 0	- I C H 7 - H D A / R G M I I / S P I / P C I / R T C / M I S C 2	
1 1	- I C H 7 - P W R / G N D	
1 2	- C L K G E N I C S 9 L P R S 5 2 5	
1 3	- D D R 2 D I M M 1 , 2	
1 4	- D D R 2 T E R M I N A T I O N	
1 5	- P C I E 1 6 x / 1 x S l o t	
1 6	- P C I S l o t	
1 7	- V G A (R G B)	
1 8	- U S B	
1 9	- P C I E L A N (R T L 8 1 1 1 D L & 8 1 0 2 E L)	
2 0	- A u d i o C o d e r c (R e a l t e k A L C 6 6 2 V C / 8 8 8)	
2 1	- A u d i o I n t e r f a c e (3 P o r t H D A)	
2 2	- D V I I n t e r f a c e	
2 3	- S u p e r I / O (I T E 8 7 1 3)	
2 4	- K B / M S / H O L E	
2 5	- C O M / L P T / R i n g / 1 0 4 L e v e l B O M	
2 6	- H M / F a n	
2 7	- V o l t a g e R e g u l a t o r	
2 8	- D u a l P o w e r	
2 9	- V R D 1 1 . 1 (u P 6 2 0 2)	
3 0	- A T X / P A N E L	





Close to CPU 12-mil width minimum



Please Close CPU

(1.5V)

H_VCCPLL

VCC1_5

FB41

FB600-06

MC9

10U-08

BC3

1U-04

10-15 mil trace

10-15 mil trace

Near CPU no more than 1.5"

根據 Chipset 需求而定
GTL_SEL1:2=11 -> 0.667VTT
GTL_SEL1:2=10 -> 0.650VTT
GTL_SEL1:2=01 -> 0.630VTT
GTL_SEL1:2=00 -> 0.615VTT

GTL Level Choice
By Chipset

8 mil trace

Put left and close to the CPU.

Put up and close to the CPU.

LGA-775P-S

CPU J3

CPU E5

CPU A24

Option for future CPU (Kentsfield)

TEST HI 9

TEST HI 8

TEST HI 7

TEST HI 6

TEST HI 5

TEST HI 4

TEST HI 3

TEST HI 2

TEST HI 1

TEST HI 0

TEST HI 0.1

TEST HI 0.2

TEST HI 0.3

TEST HI 0.4

TEST HI 0.5

TEST HI 0.6

TEST HI 0.7

TEST HI 0.8

TEST HI 0.9

TEST HI 1.0

TEST HI 1.1

TEST HI 1.2

TEST HI 1.3

TEST HI 1.4

TEST HI 1.5

TEST HI 1.6

TEST HI 1.7

TEST HI 1.8

TEST HI 1.9

TEST HI 2.0

TEST HI 2.1

TEST HI 2.2

TEST HI 2.3

TEST HI 2.4

TEST HI 2.5

TEST HI 2.6

TEST HI 2.7

TEST HI 2.8

TEST HI 2.9

TEST HI 3.0

TEST HI 3.1

TEST HI 3.2

TEST HI 3.3

TEST HI 3.4

TEST HI 3.5

TEST HI 3.6

TEST HI 3.7

TEST HI 3.8

TEST HI 3.9

TEST HI 4.0

TEST HI 4.1

TEST HI 4.2

TEST HI 4.3

TEST HI 4.4

TEST HI 4.5

TEST HI 4.6

TEST HI 4.7

TEST HI 4.8

TEST HI 4.9

TEST HI 5.0

TEST HI 5.1

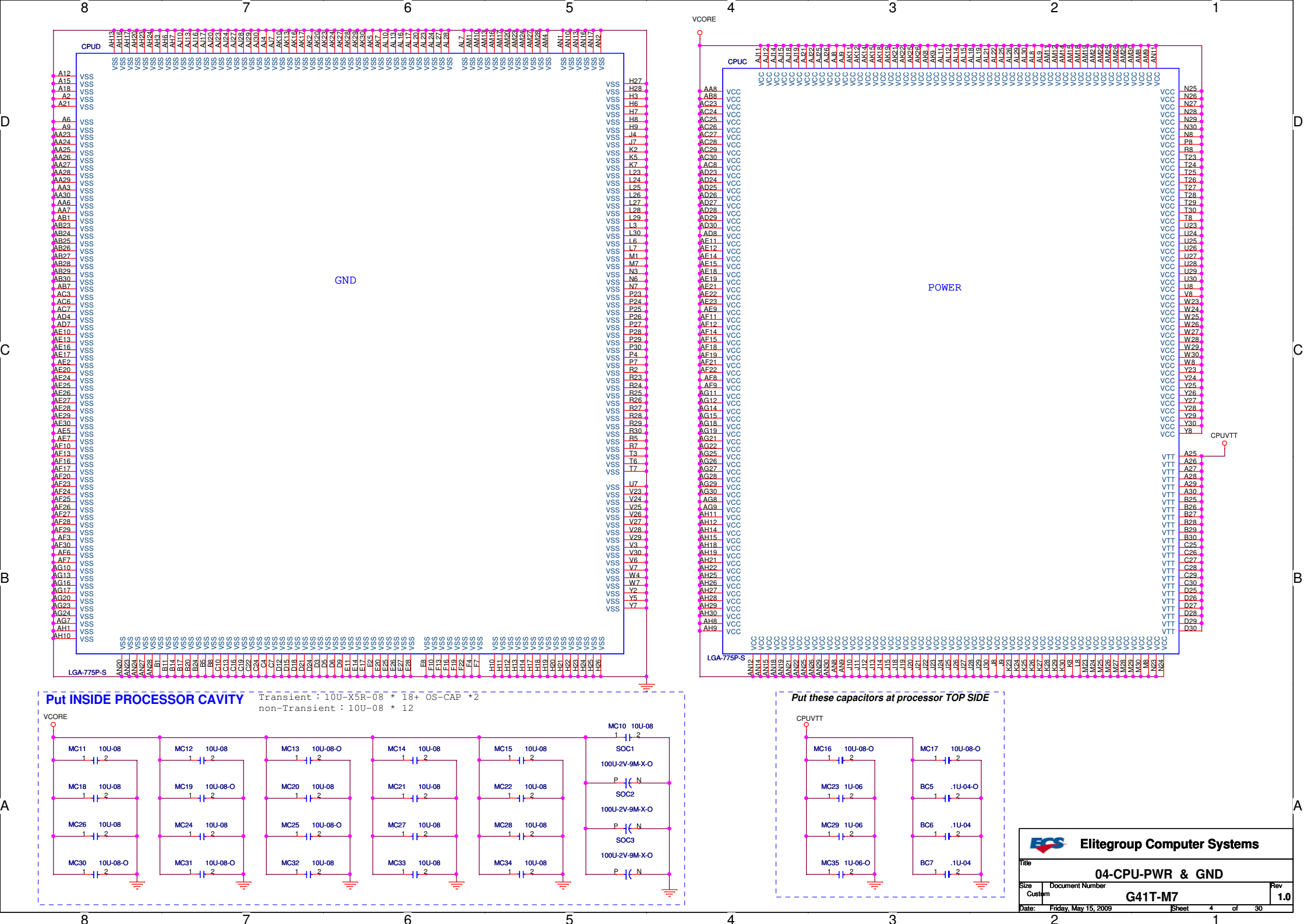
TEST HI 5.2

TEST HI 5.3

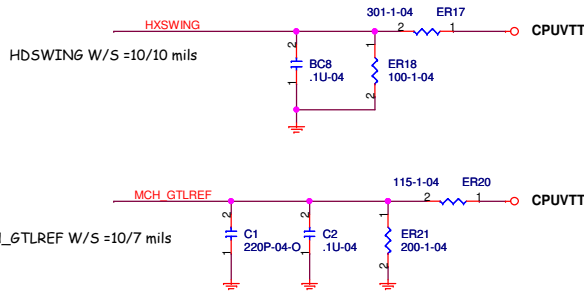
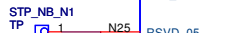
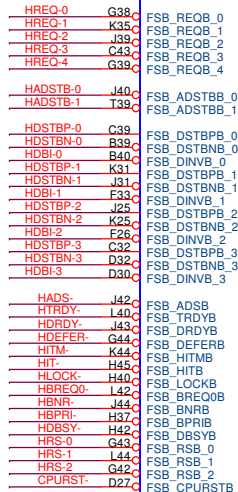
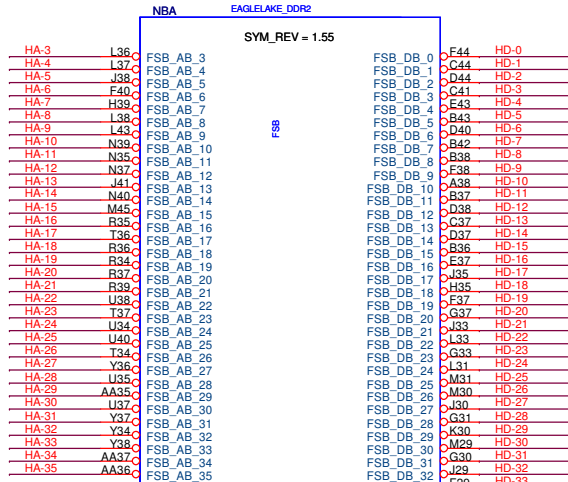
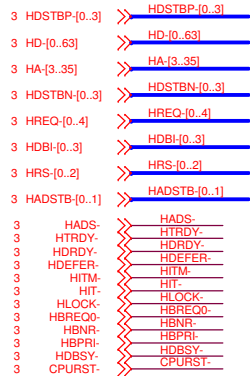
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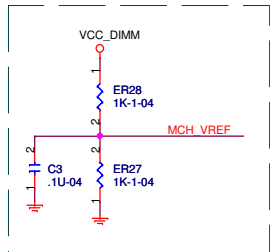
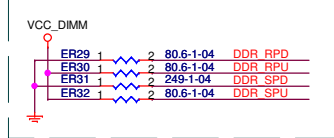
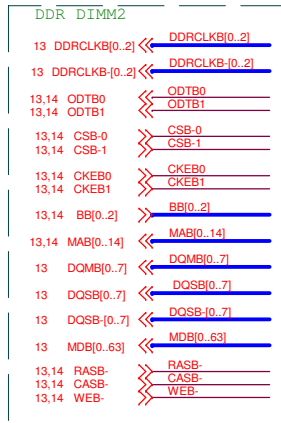
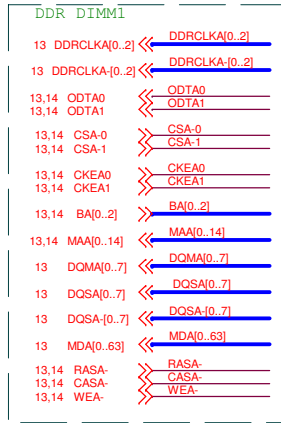
TEST HI 5.5

TEST HI 5.6



HOST





NBC EAGLELAKE_DDR2

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MAA1	BC35	DDR_A_MA_1	DDR_A_DQS_0	BD4	DQSA-0
MAA2	BB32	DDR_A_MA_2	DDR_A_MA_2	BC3	DQMA0
MAA3	BC32	DDR_A_MA_3	DDR_A_DM_0		
MAA4	BB32	DDR_A_MA_4	DDR_A_DQ_0	BC2	MDA0
MAA5	BB31	DDR_A_MA_5	DDR_A_DQ_1	BD3	MDA1
MAA6	AY31	DDR_A_MA_6	DDR_A_DQ_2	BD7	MDA2
MAA7	BA31	DDR_A_MA_7	DDR_A_DQ_3	BB7	MDA3
MAA8	BD31	DDR_A_MA_8	DDR_A_DQ_4	BB2	MDA4
MAA9	BD30	DDR_A_MA_9	DDR_A_DQ_5	BA3	MDA5
MAA10	AW43	DDR_A_MA_10	DDR_A_DQ_6	BE6	MDA6
MAA11	BC30	DDR_A_MA_11	DDR_A_DQ_7	BD6	MDA7
MAA12	BB30	DDR_A_MA_12			
MAA13	AM42	DDR_A_MA_13	DDR_A_DQS_1	BB9	DQSA1
MAA14	BD28	DDR_A_MA_14	DDR_A_DQS_1	BC9	DQSA-1
			DDR_A_DM_1	BD9	DQMA1
WEA-	AW42	DDR_A_WEB	DDR_A_DQ_8	BB8	MDA8
CASA-	AU42	DDR_A_CASB	DDR_A_DQ_9	AY8	MDA9
RASA-	AY42	DDR_A_RASB	DDR_A_DQ_10	BD11	MDA10
			DDR_A_DQ_11	BB11	MDA11
BA0	AV45	DDR_A_BS_0	DDR_A_DQ_12	BC7	MDA12
BA1	AY44	DDR_A_BS_1	DDR_A_DQ_13	BE8	MDA13
BA2	BC28	DDR_A_BS_2	DDR_A_DQ_14	BD10	MDA14
			DDR_A_DQ_15	AY11	MDA15
CSA-0	AU43	DDR_A_CSB_0	DDR_A_DQS_2	BD15	DQSA2
CSA-1	AR40	DDR_A_CSB_1	DDR_A_DQS_2	BB15	DQSA-2
	AU43	DDR_A_CSB_2	DDR_A_DM_2	BD14	DQMA2
	AM43	DDR_A_CSB_3			
CKEA0	BB27	DDR_A_CKE_0	DDR_A_DQ_16	BB14	MDA16
RASA-	BD27	DDR_A_CKE_1	DDR_A_DQ_17	BC14	MDA17
CASA-	BA27	DDR_A_CKE_2	DDR_A_DQ_18	BC16	MDA18
WEA-	AY28	DDR_A_CKE_3	DDR_A_DQ_19	BB16	MDA19
			DDR_A_DQ_20	BC11	MDA20
ODTA0	AR42	DDR_A_ODT_0	DDR_A_DQ_21	BE12	MDA21
ODTA1	AM44	DDR_A_ODT_1	DDR_A_DQ_22	BA15	MDA22
	AR44	DDR_A_ODT_2	DDR_A_DQ_23	BD16	MDA23
	AL40	DDR_A_ODT_3			
DDRCLKA0	AY37	DDR_A_CK_0	DDR_A_DQS_3	AR22	DQSA3
DDRCLKA-0	BA37	DDR_A_CK_0	DDR_A_DQS_3	AT22	DQSA-3
DDRCLKA1	AW29	DDR_A_CK_1	DDR_A_DM_3	AV22	DQMA3
DDRCLKA2	AY29	DDR_A_CK_2			
DDRCLKA-2	AU37	DDR_A_CK_2	DDR_A_DQ_24	AW21	MDA24
	AV37	DDR_A_CK_2	DDR_A_DQ_25	AY22	MDA25
	AT33	DDR_A_CK_3	DDR_A_DQ_26	AV24	MDA26
	AT30	DDR_A_CK_3	DDR_A_DQ_27	AY24	MDA27
	AR30	DDR_A_CK_4	DDR_A_DQ_28	AU21	MDA28
	AW38	DDR_A_CK_4	DDR_A_DQ_29	AT21	MDA29
	AY38	DDR_A_CK_5	DDR_A_DQ_30	AR24	MDA30
			DDR_A_DQ_31	AU24	MDA31
			DDR_A_DQS_4	AH43	DQSA4
			DDR_A_DQS_4	AH42	DQSA-4
			DDR_A_DM_4	AK42	DQMA4
			DDR_A_DQ_32	AL41	MDA32
			DDR_A_DQ_33	AK43	MDA33
			DDR_A_DQ_34	AG42	MDA34
			DDR_A_DQ_35	AG44	MDA35
			DDR_A_DQ_36	AL42	MDA36
			DDR_A_DQ_37	AK44	MDA37
			DDR_A_DQ_38	AH44	MDA38
			DDR_A_DQ_39	AG41	MDA39
			DDR_A_DQS_5	AD43	DQSA5
			DDR_A_DQS_5	AE42	DQSA-5
			DDR_A_DM_5	AE45	DQMA5
			DDR_A_DQ_40	AF43	MDA40
			DDR_A_DQ_41	AF42	MDA41
			DDR_A_DQ_42	AC44	MDA42
			DDR_A_DQ_43	AF40	MDA43
			DDR_A_DQ_44	AF44	MDA44
			DDR_A_DQ_45	AE44	MDA45
			DDR_A_DQ_46	AD44	MDA46
			DDR_A_DQ_47	AC41	MDA47
			DDR_A_DQS_6	Y43	DQSA6
			DDR_A_DQS_6	Y42	DQSA-6
			DDR_A_DM_6	AA45	DQMA6
			DDR_A_DQ_48	AB43	MDA48
			DDR_A_DQ_49	AA42	MDA49
			DDR_A_DQ_50	W42	MDA50
			DDR_A_DQ_51	W41	MDA51
			DDR_A_DQ_52	AB42	MDA52
			DDR_A_DQ_53	AF40	MDA53
			DDR_A_DQ_54	Y44	MDA54
			DDR_A_DQ_55	Y40	MDA55
			DDR_A_DQS_7	T44	DQSA7
			DDR_A_DQS_7	T43	DQSA-7
			DDR_A_DM_7	T42	DQMA7
			DDR_A_DQ_56	V42	MDA56
			DDR_A_DQ_57	U45	MDA57
			DDR_A_DQ_58	R40	MDA58
			DDR_A_DQ_59	P44	MDA59
			DDR_A_DQ_60	V44	MDA60
			DDR_A_DQ_61	V43	MDA61
			DDR_A_DQ_62	R41	MDA62
			DDR_A_DQ_63	R44	MDA63

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NBD EAGLELAKE_DDR2

SYM_REV = 1.55

MAB0	BD24	DDR_B_MA_0	DDR_B_DQS_0	AW8	DQSB0
MAB1	BB23	DDR_B_MA_1	DDR_B_DQS_0	AW9	DQSB-0
MAB2	BB24	DDR_B_MA_2	DDR_B_DM_0	AY6	DQMB0
MAB3	BD23	DDR_B_MA_3			
MAB5	BB22	DDR_B_MA_4	DDR_B_DQ_0	AV7	MDB0
MAB6	BC22	DDR_B_MA_5	DDR_B_DQ_1	AW4	MDB1
MAB7	BC20	DDR_B_MA_6	DDR_B_DQ_2	BA9	MDB2
MAB8	BB20	DDR_B_MA_7	DDR_B_DQ_3	AU11	MDB3
MAB9	BD20	DDR_B_MA_8	DDR_B_DQ_4	AU7	MDB4
MAB10	BC26	DDR_B_MA_9	DDR_B_DQ_5	AU8	MDB5
MAB11	BD19	DDR_B_MA_10	DDR_B_DQ_6	AW7	MDB6
MAB12	BB19	DDR_B_MA_11	DDR_B_DQ_7	AY9	MDB7
MAB13	BE38	DDR_B_MA_12	DDR_B_DQS_1	AT15	DQSB1
MAB14	BA19	DDR_B_MA_13	DDR_B_DQS_1	AU15	DQSB-1
		DDR_B_MA_14	DDR_B_DM_1	AR15	DQMB1
WEB-	BD36	DDR_B_WEB	DDR_B_DQ_8	AY13	MDB8
CASB-	BC37	DDR_B_CASB	DDR_B_DQ_9	AP15	MDB9
RASB-	BD35	DDR_B_RASB	DDR_B_DQ_10	AW15	MDB10
			DDR_B_DQ_11	AT16	MDB11
BB0	BD26	DDR_B_BS_0	DDR_B_DQ_12	AU13	MDB12
BB1	BB26	DDR_B_BS_1	DDR_B_DQ_13	AW13	MDB13
BB2	BD18	DDR_B_BS_2	DDR_B_DQ_14	AP16	MDB14
			DDR_B_DQ_15	AU16	MDB15
CSB-0	BB35	DDR_B_CSB_0	DDR_B_DQS_2	AR20	DQSB2
CSB-1	BD39	DDR_B_CSB_1	DDR_B_DQS_2	AR17	DQSB-2
	BB37	DDR_B_CSB_2	DDR_B_DM_2	AU17	DQMB2
	BD40	DDR_B_CSB_3			
CKEB0	BC18	DDR_B_CKE_0	DDR_B_DQ_16	AY17	MDB16
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	BB38	DDR_B_ODT_2	DDR_B_DQ_22	AT20	MDB22
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			DDR_B_DQS_3	AT26	DQSB-3
			DDR_B_DM_3	AV25	DQMB3
			DDR_B_DQ_24	AT25	MDB24
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			DDR_B_DQ_29	AR25	MDB29
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			DDR_B_DQS_4	AR37	DQSB-4
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			DDR_B_DQ_37	AW39	MDB37
			DDR_B_DQ_38	AU40	MDB38
			DDR_B_DQ_39	AU41	MDB39
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			DDR_B_DQS_5	AL34	DQSB-5
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			DDR_B_DQS_7	AD35	DQSB-7
			DDR_B_DM_7	AD37	DQMB7
			DDR_B_DQ_56	AD40	MDB56
			DDR_B_DQ_57	AD38	MDB57
			DDR_B_DQ_58	AB40	MDB58
			DDR_B_DQ_59	AA39	MDB59
			DDR_B_DQ_60	AE36	MDB60
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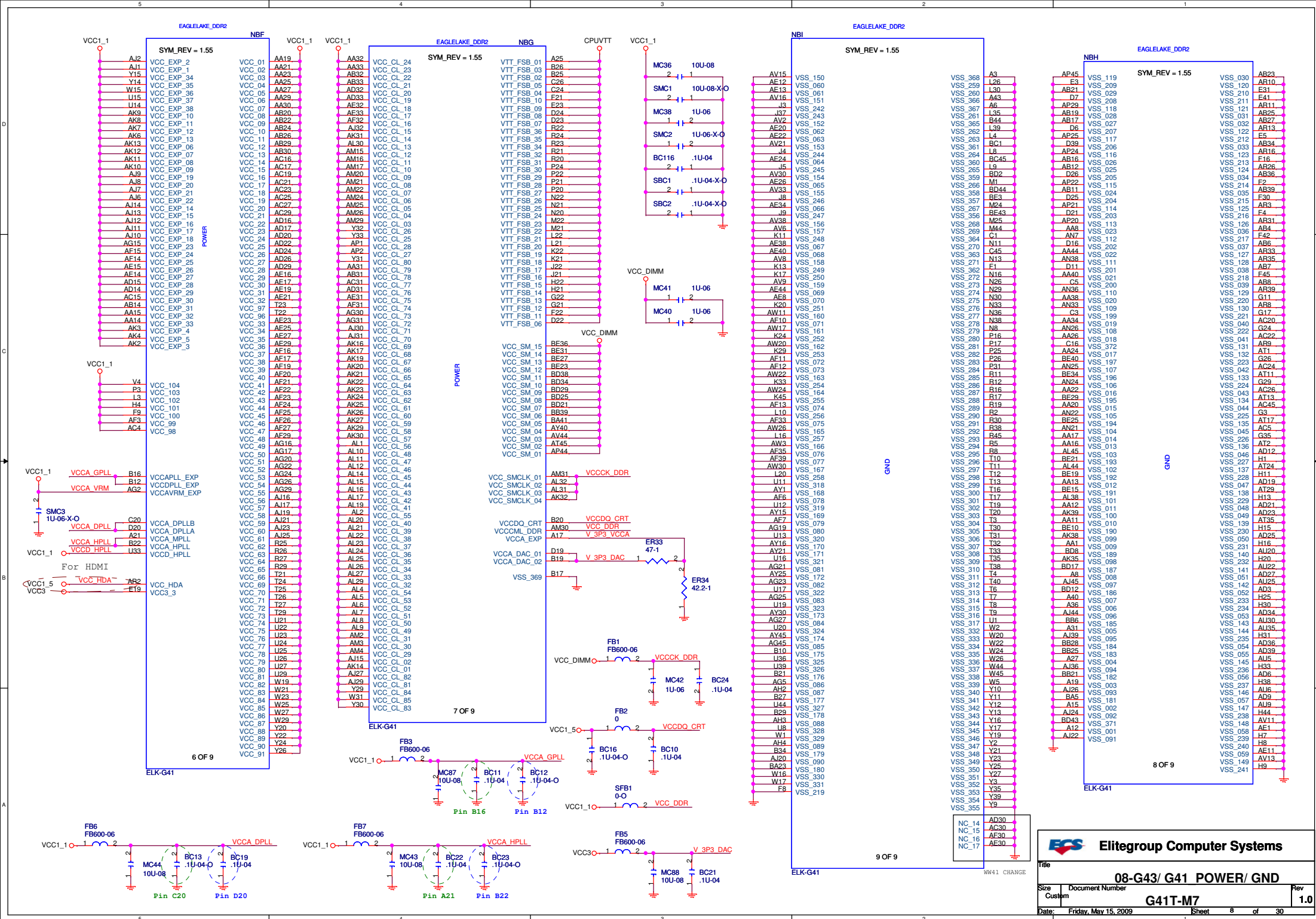
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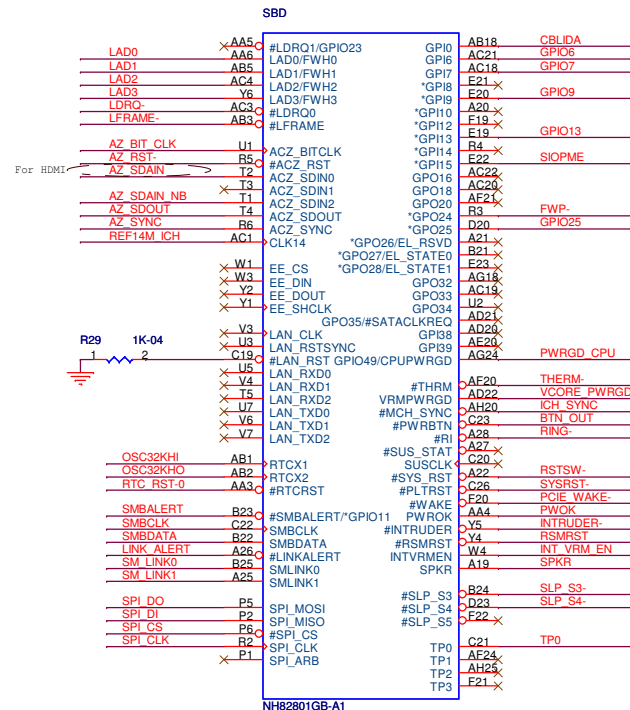
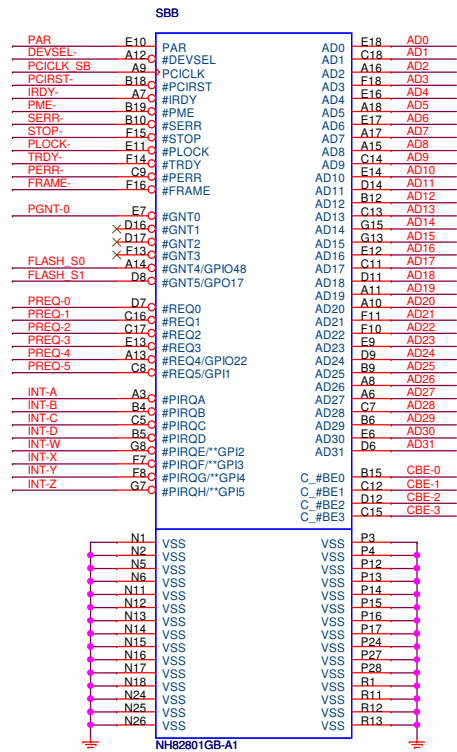
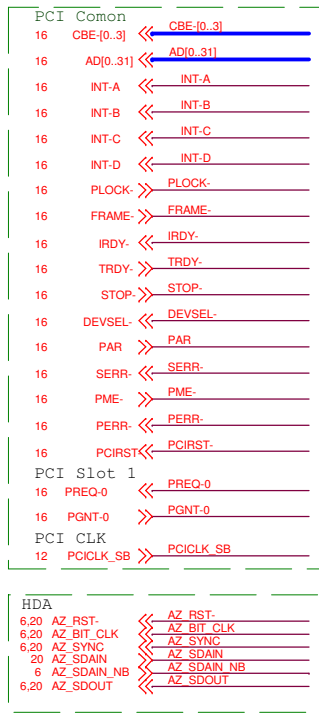
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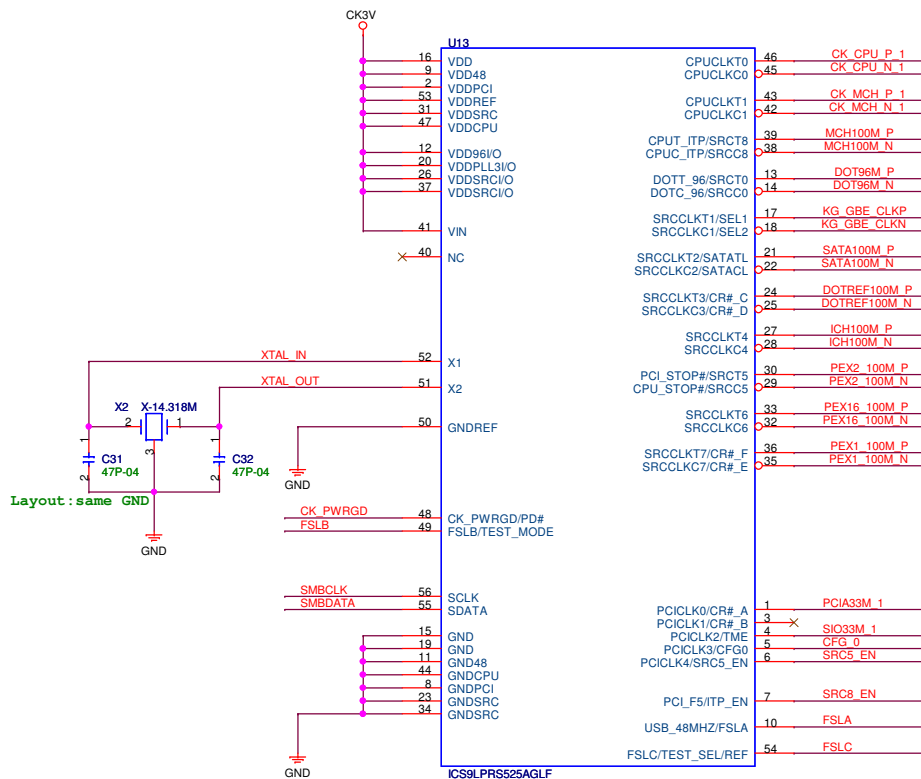
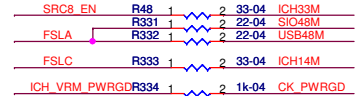
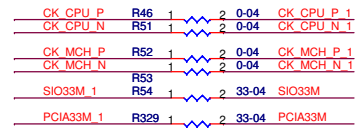
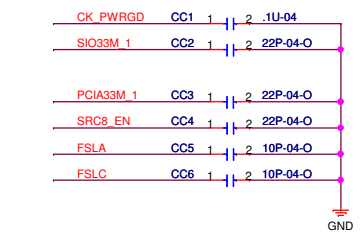
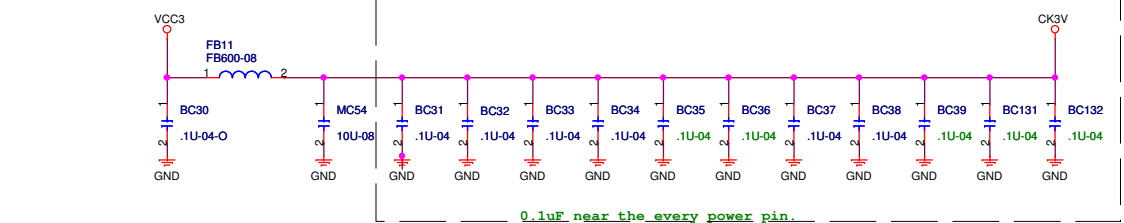
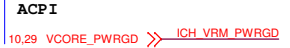
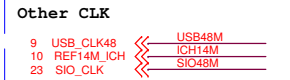
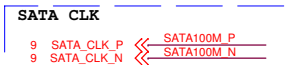
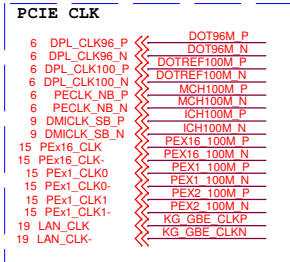
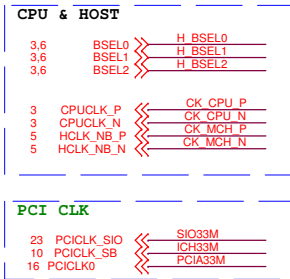
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Size Document Number G41T-M7 Rev 1.0

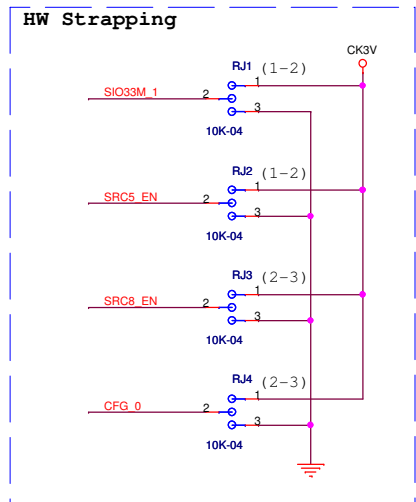
Date: Friday, May 15, 2009 Sheet 7 of 30







- CPU
- MCH (FSB)
- MCH (PCIE)
- MCH (VGA)
- LAN
- ICH (SATA)
- MCH (DIGITAL VIDEO)
- ICH
- X1
- X16
- X1



Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU CLOCK (MHZ)	CPU FSB CLOCK
0	0	0	266.66	FSB 1066
0	1	0	200.00	FSB 800
1	0	0	333.33	FSB 1333

FOR ICS9LPRS525AGLF
PIN 4(TIME)STRAP

PIN 4 (TIME)	
HI	Overclocking of CPU and SRC NOT allowed
LO	Overclocking of CPU and SRC allowed

FOR ICS9LPRS525AGLF
PIN 5(CFG0)STRAP

PIN 5 (CFG0)	PIN 4 (TIME)	PCI3/CFG0 PLL Mode
LO	X	0
MID	X	1
HI	TME=0	2
HI	TME=1	3

Don't select PLL mode 3,
it's will effect LAN frequency

FOR ICS9LPRS525AGLF
PIN 6(SRC5_EN)STRAP

PIN 6 (SRC5_EN)	PIN 29,30
HI	SRC FUNCTION
LO	CPU & PCI STOP #

FOR ICS9LPRS525AGLF
PIN 7(ITP_EN)STRAP

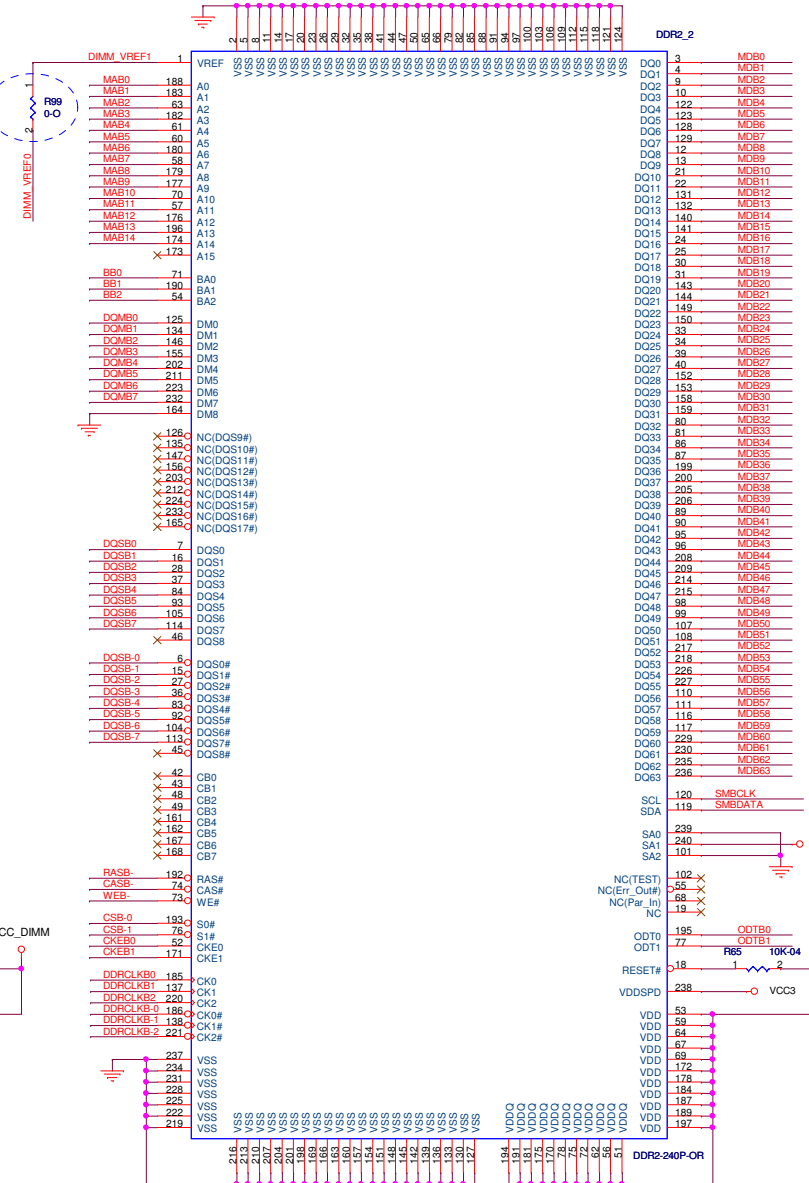
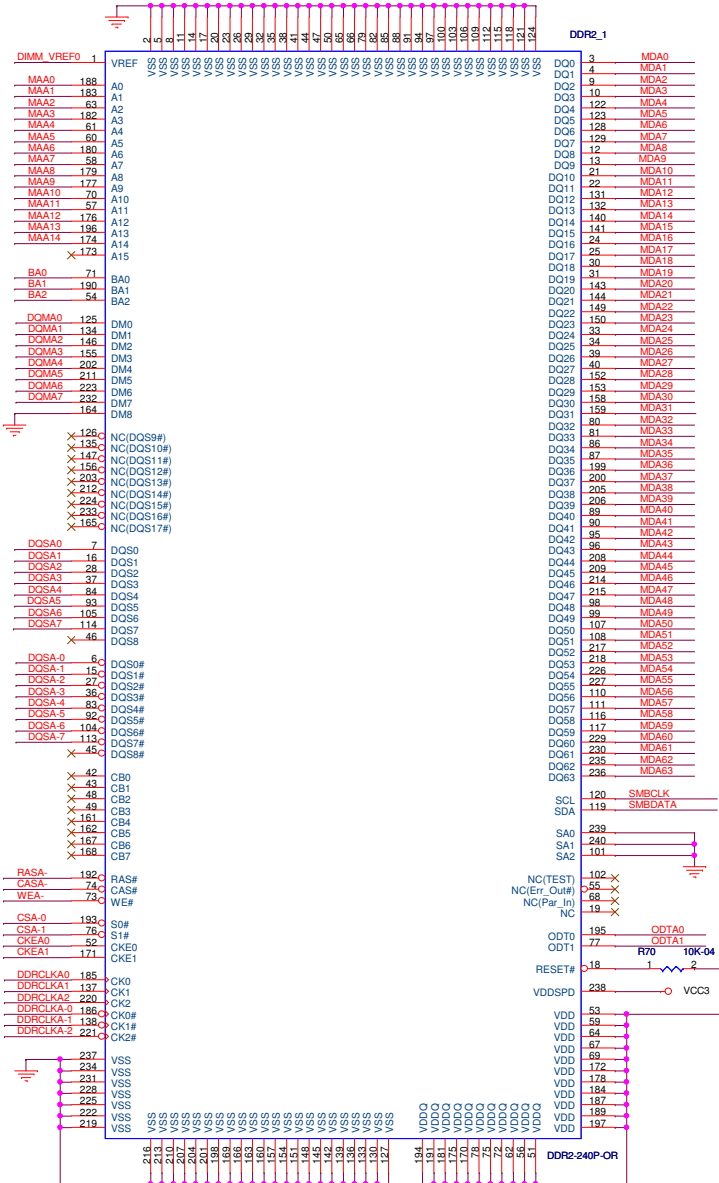
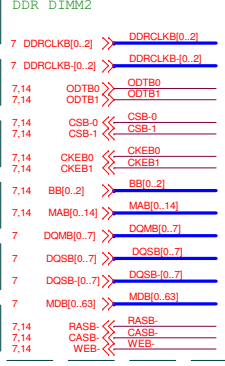
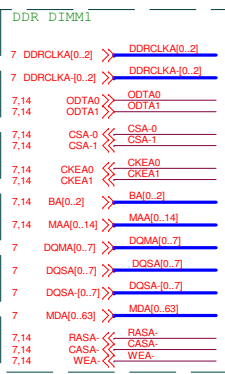
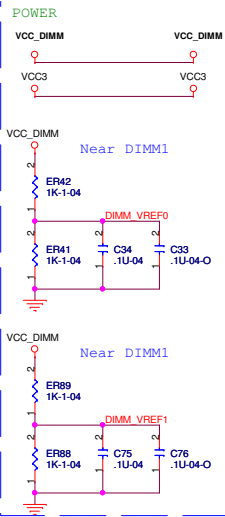
PIN 7 (ITP_EN)	PIN 38,39 MODE
HI	CPU ITP FUNCTION
LO	SRC8

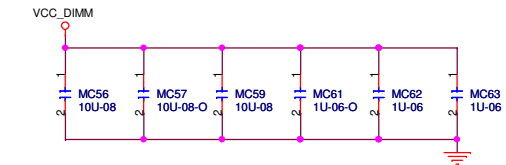
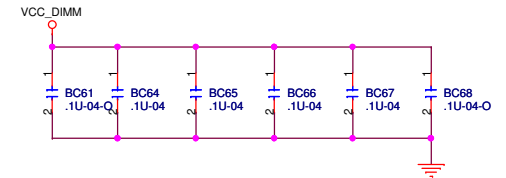
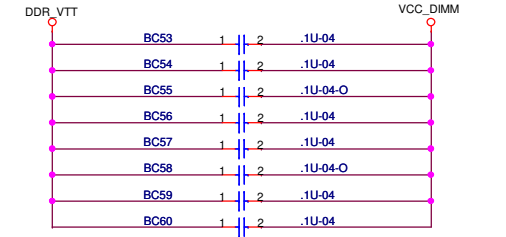
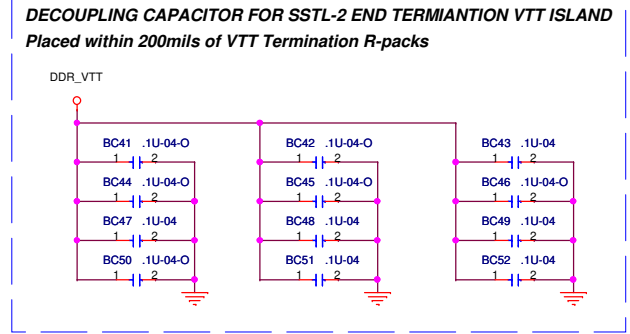
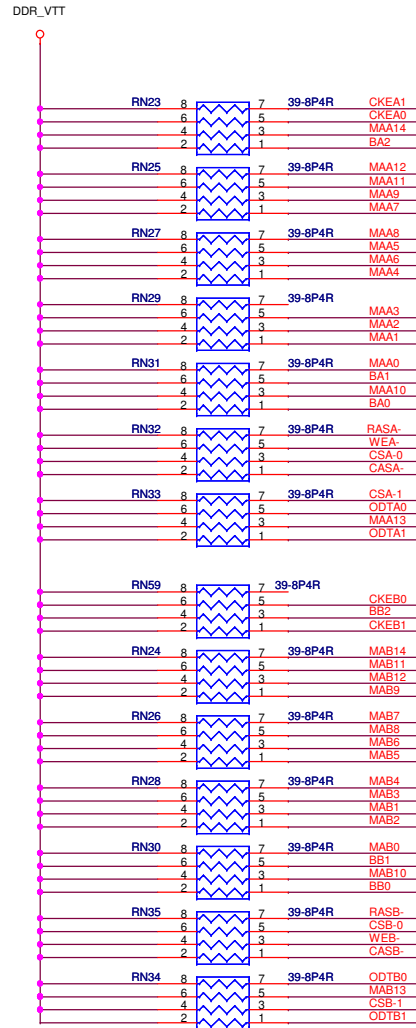
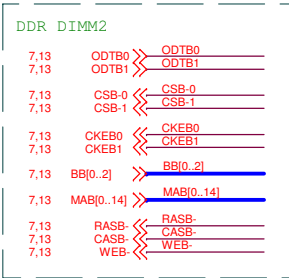
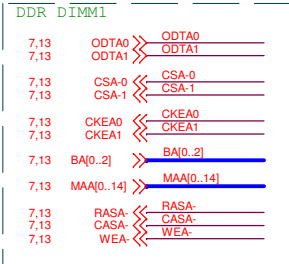
Elitegroup Computer Systems

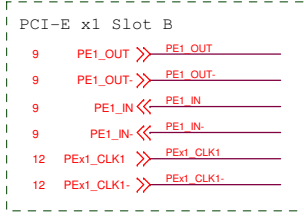
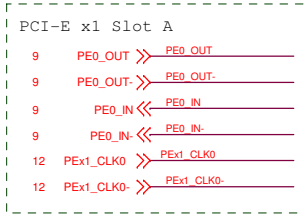
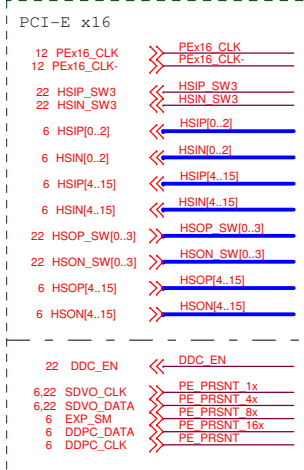
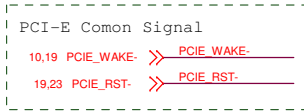
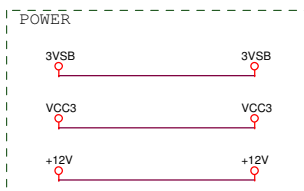
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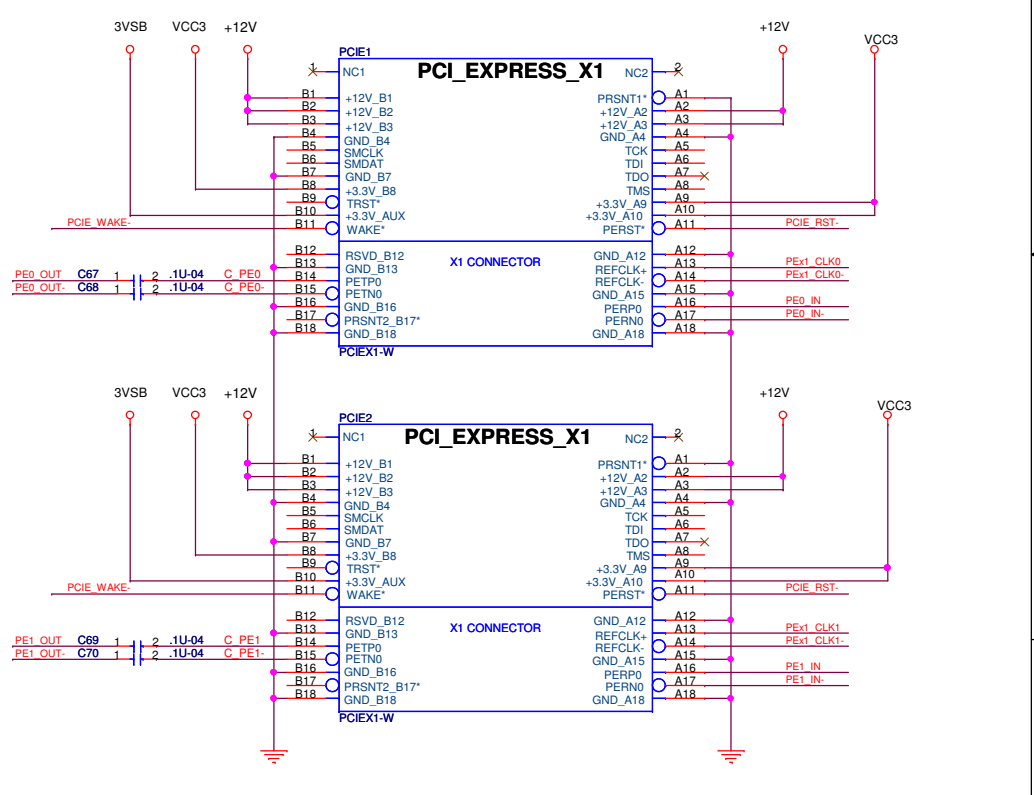
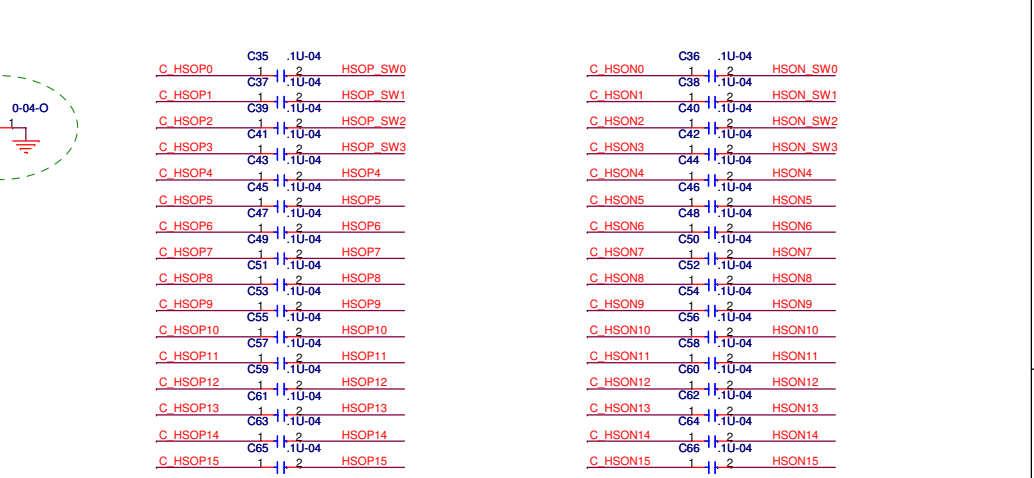
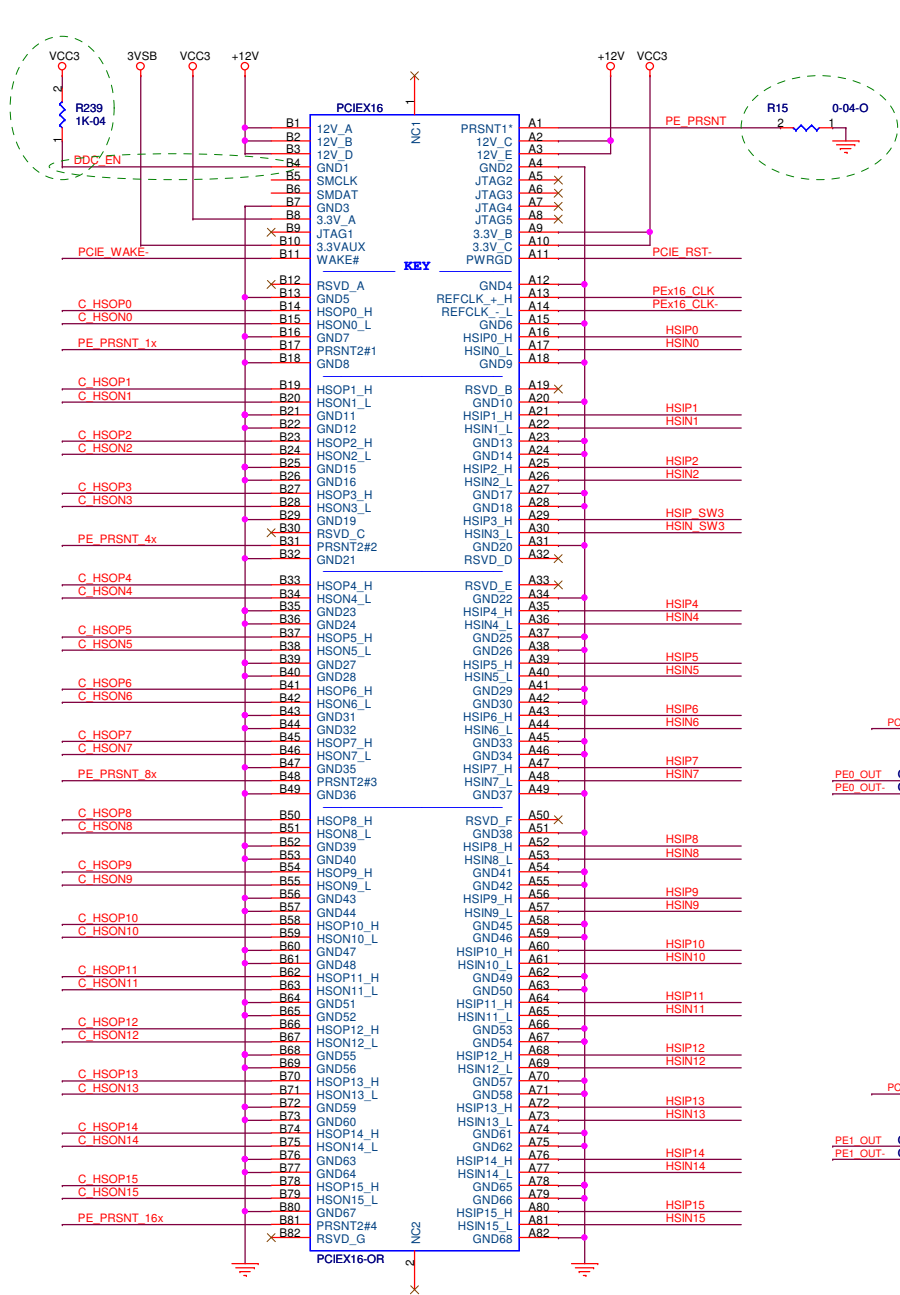
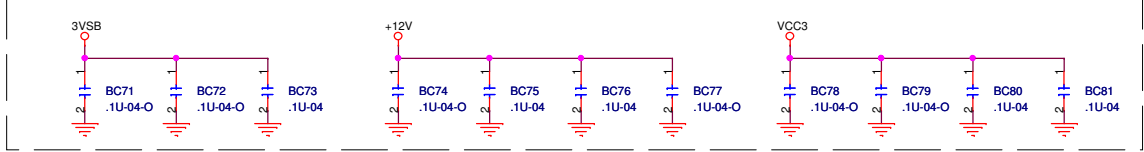
Date: Friday, May 15, 2009 Sheet 12 of 30



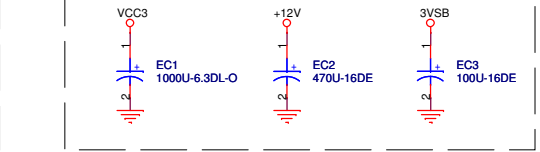


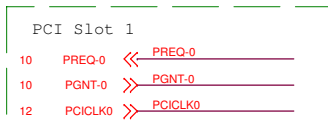


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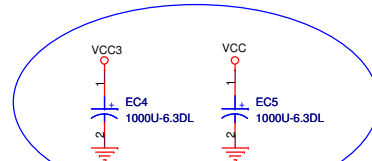
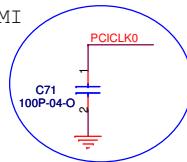
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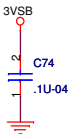
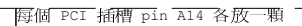
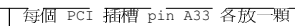
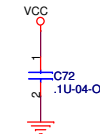
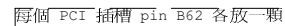
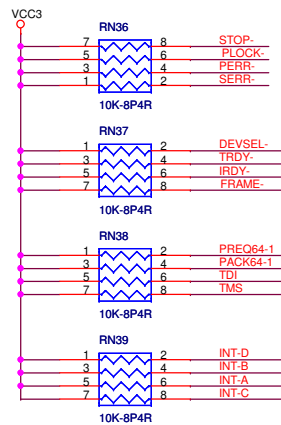


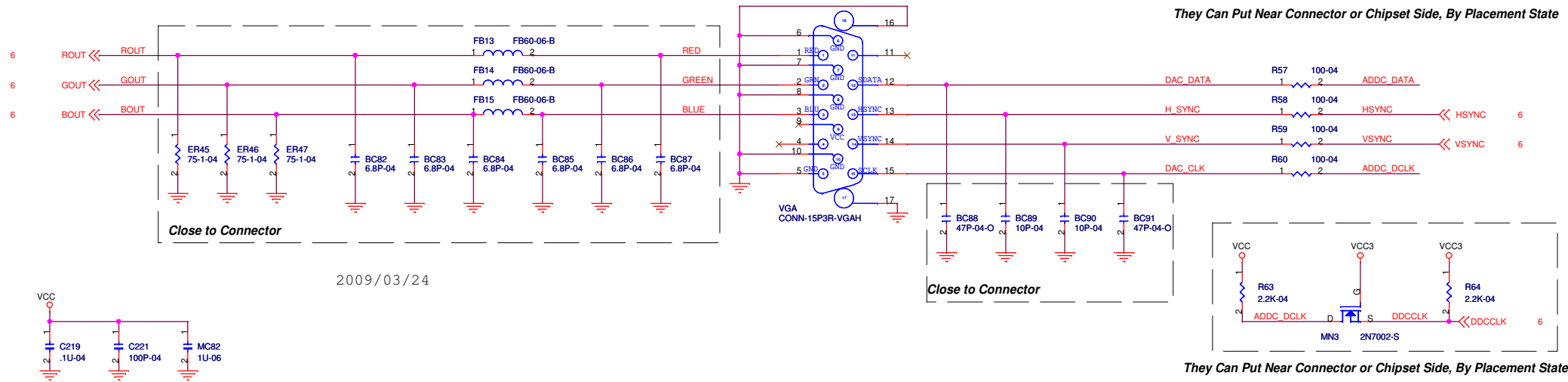
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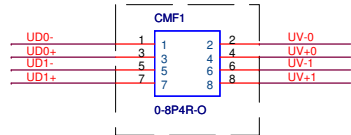
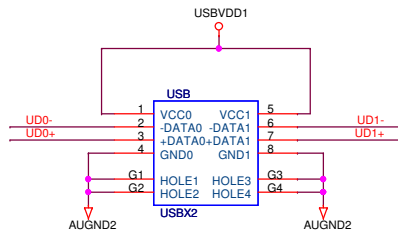
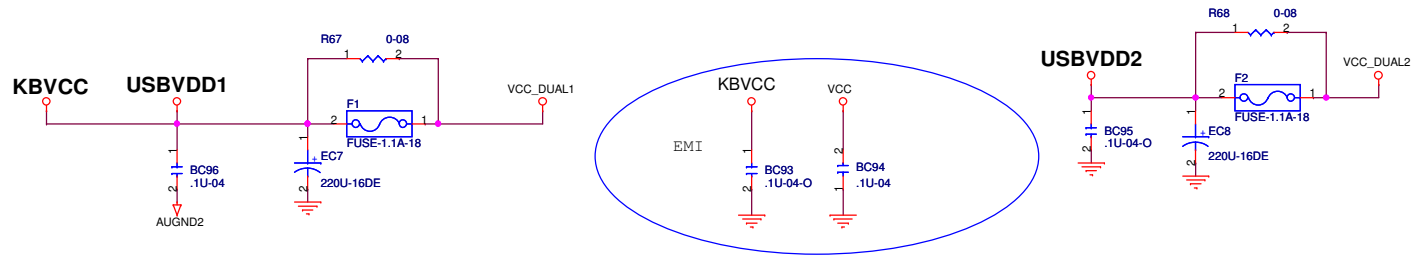
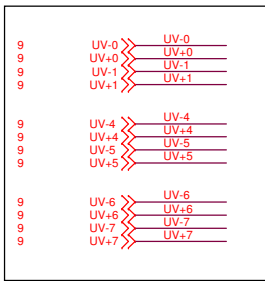
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INT [A, B, C, D]
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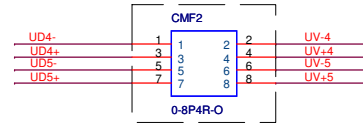
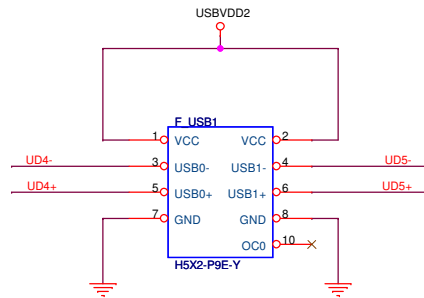
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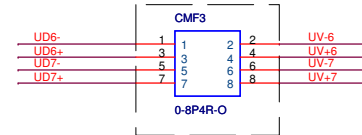
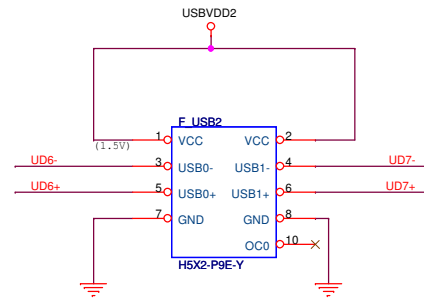




Close to USB connector



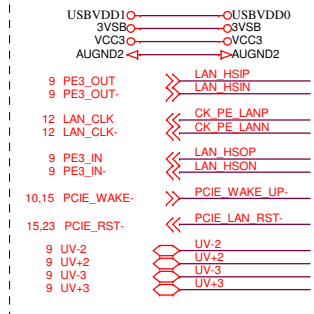
Close to header(F_USB1)



Close to header(F_USB2)



External Connection



When you found some bug, please inform Ren(ext:665) to update circuit.

新手提醒:

- LAN_HSOP/N請接到SB的PCIE RX端
- LAN_HSIP/N請接到SB的PCIE TX端
- LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

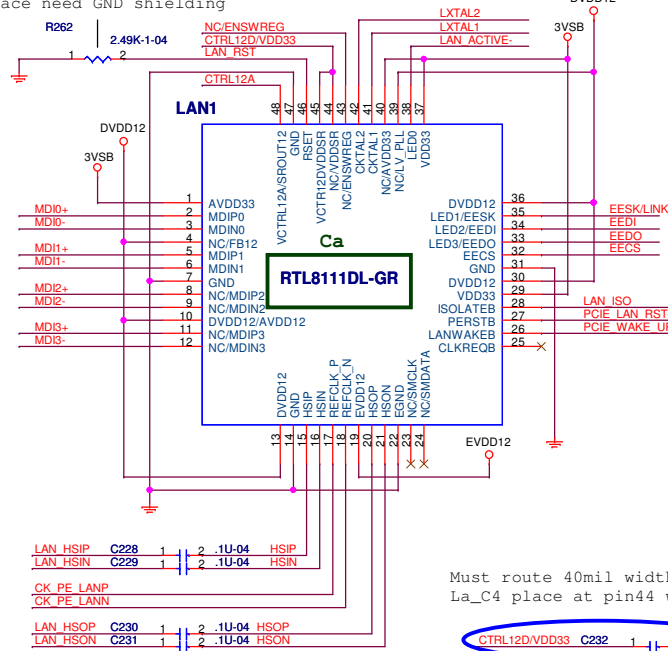
BOM Difference

	RTL8111DL-GR 1000M	RTL8102EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8102EL-GR
Cb	X	V
Cc	0-04	.01U-04
Cd	X	V
Ce	V	X
Cf	USBX2-LAN-1000	USBX2-LAN-100

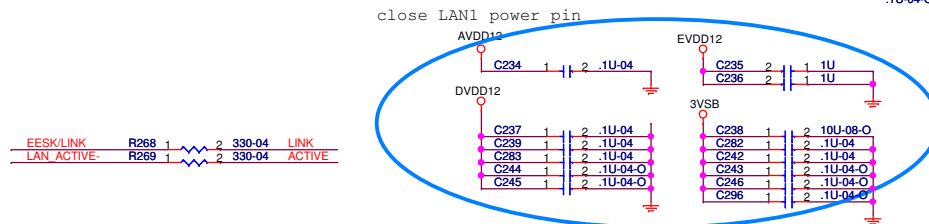
Power Difference

	RTL8111D	RTL8102E
AVDD33	3.3V	3.3V
VDD33	3VSB供應	3VSB供應
CTRL12A	Switching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應

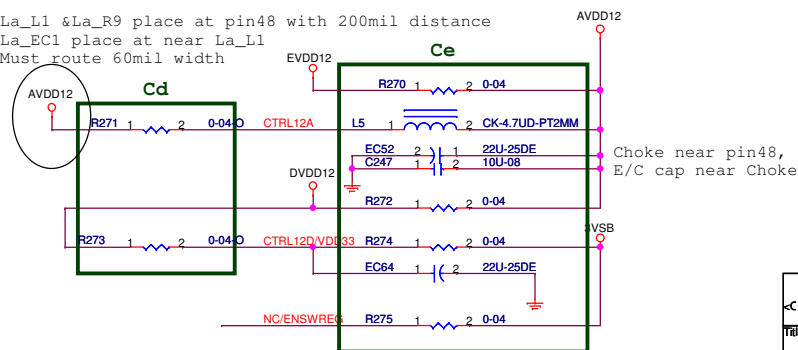
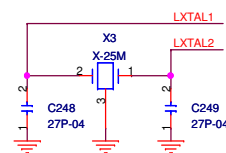
RSET電阻需close to LAN
Trace need GND shielding



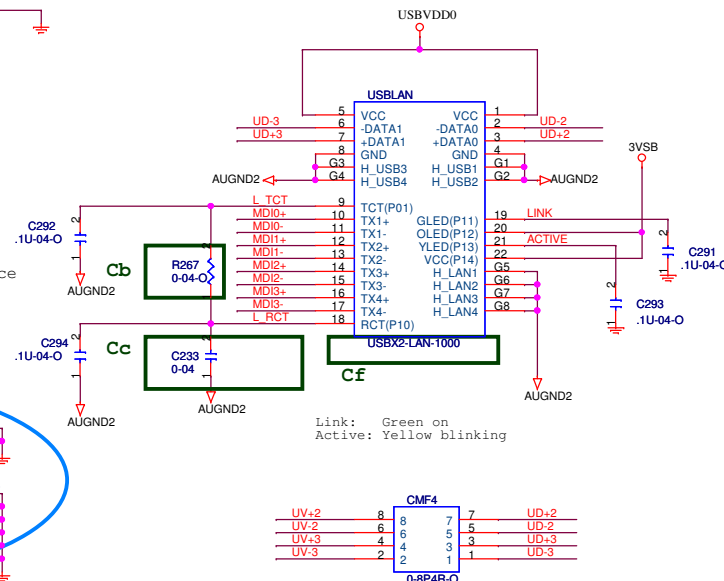
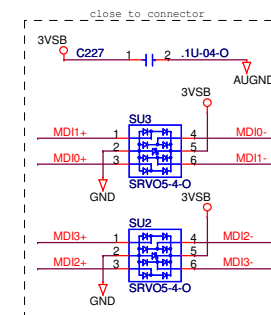
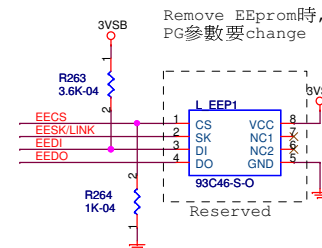
Must route 40mil width
La_C4 place at pin44 with 200mil distance



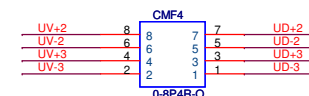
La_L1 & La_R9 place at pin48 with 200mil distance
La_EC1 place at near La_L1
Must route 60mil width



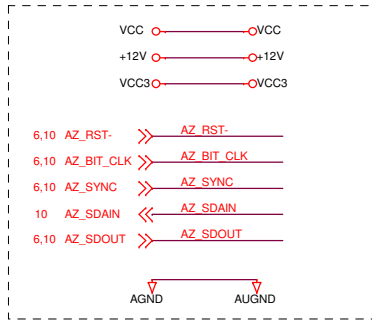
Remove EEprom時,
PG參數要change



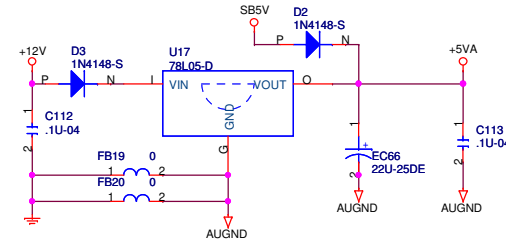
Link: Green on
Active: Yellow blinking



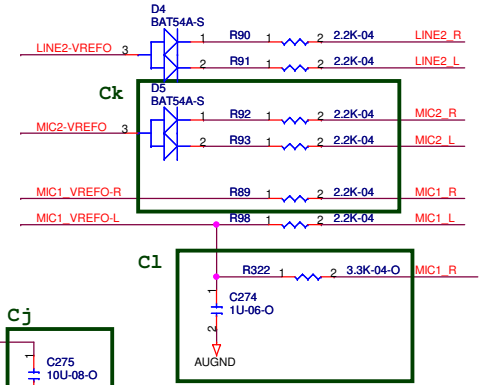
External Connection



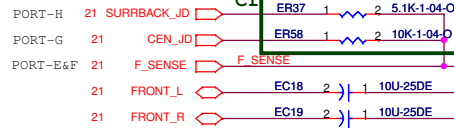
When you found some bug, please inform Ren(ext:665) to update circuit.



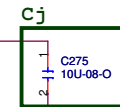
MIC Bias



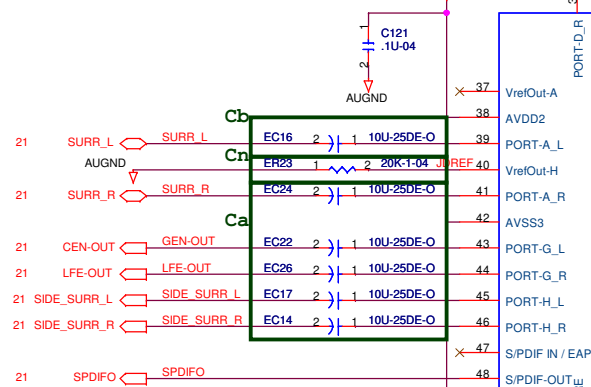
Resistors Networks



Ch



CODEC



ALC662-VC-GR

Cc

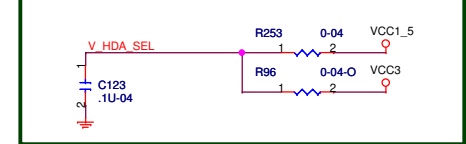


Cg

Resistors Networks



HDA Voltage Select

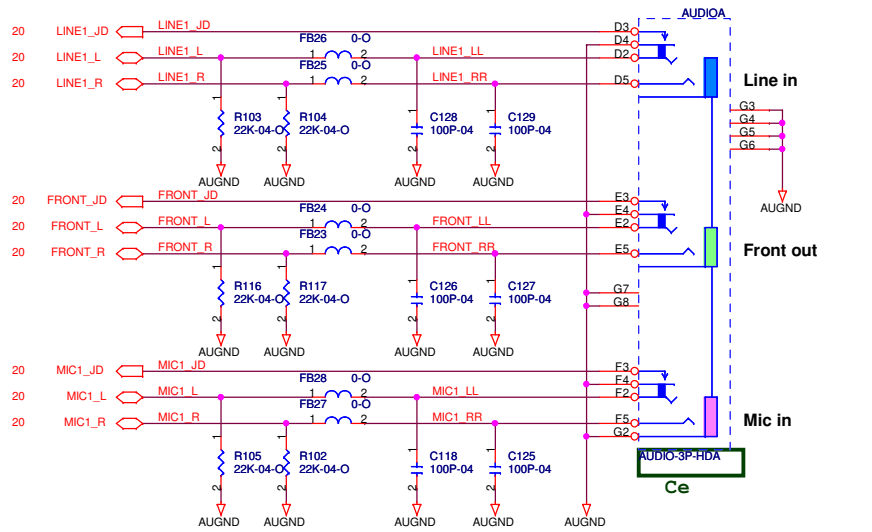


BOM Difference

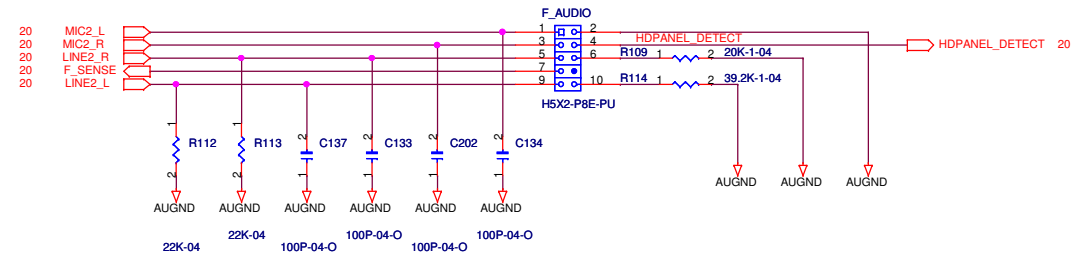
Location	ALC888VC 7.1 Ch	ALC662 5.1 CH	VT1708B 7.1CH	VT1708B 5.1CH
Ca	V	X	V	X
Cb	V	X	V	X
Cc	ALC888-GR C2S	ALC662-VC-GRS	VT1708BS	VT1708BS
Cd	V	X	V	X
Ce	AUDIO-6P	AUDIO-3P-HDA	AUDIO-6P	AUDIO-3P-HDA
Cf	V	X	V	X
Cg	V	X	V	X
Ch	V	X	V	X
Ci	V	V	X	X
Cj	X	X	V	V
Ck	V	V	X	X
Cl	X	X	V	V
Cm	VCC1.5/VCC3	VCC1.5/VCC3	VCC3	VCC3
Cn	20K-1-04	20K-1-04	5.1K-1-04	5.1K-1-04

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

REAR-AUDIO



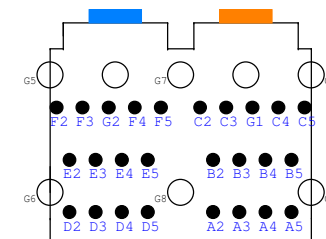
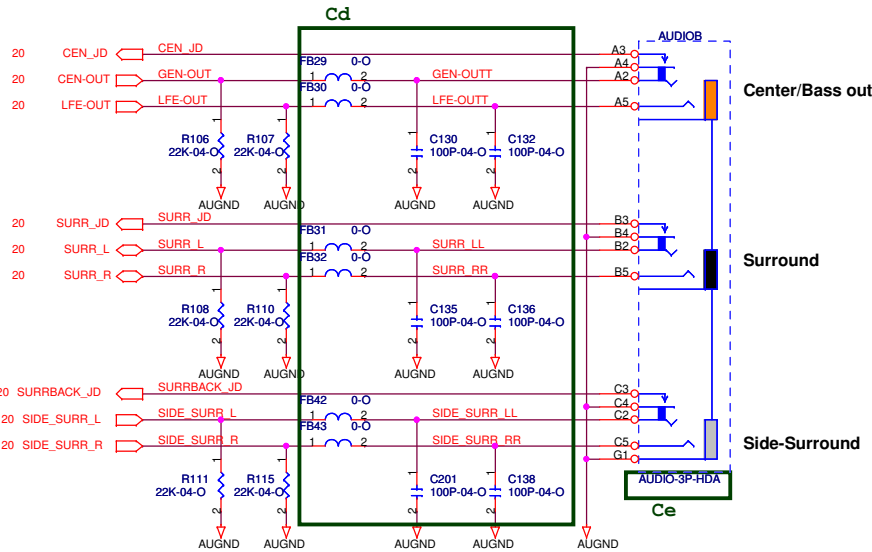
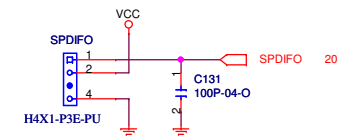
FRONT-AUDIO



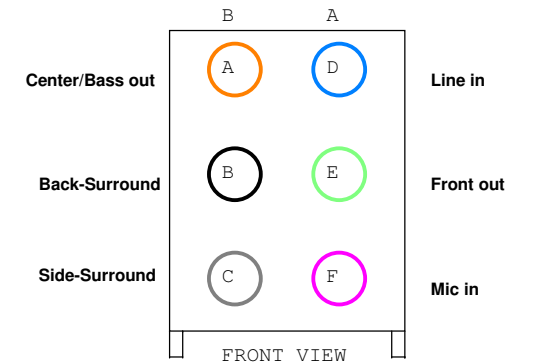
CD_IN



SPDIF-OUT



TOP VIEW



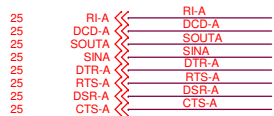
FRONT VIEW

HW Monitor

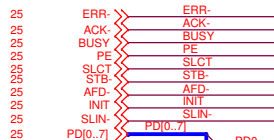


VIN0 for VCORE
VIN1 for V_DIMM
VIN2 for VCC

COM



LPT



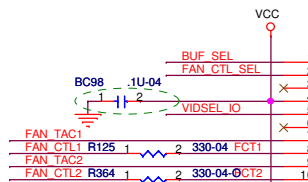
KB/MS



IT8713Power On Strapping Options

JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP2	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3	CHIP_SEL		Chip selection in Configuration
JP4	BUF_SEL	1	Output Buffer of PCIRST are open-drain
		0	Output Buffer of PCIRST are push-pull
JP5 : JP7	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 00h
		10	The default value of EC Index 15h/16h/17h is 40h
		01	The default value of EC Index 15h/16h/17h is 20h
		00	The default value of EC Index 15h/16h/17h is 7Fh
JP6	VID_SEL	1	Threshold V of VID is 2.0/0.8 V
		0	Threshold V of VID is 0.8/0.4 V
JP7	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK

DCD-A
RFA
CTS-A
DTR-A
RTS-A
DSR-A
SOUTA
SINA

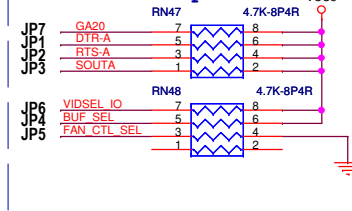


EX_GPIO_2
EX_GPIO_1
EX_GPIO_0
THERM
GTL_SEL2
GTL_SEL1
ACPILED
PWRLED

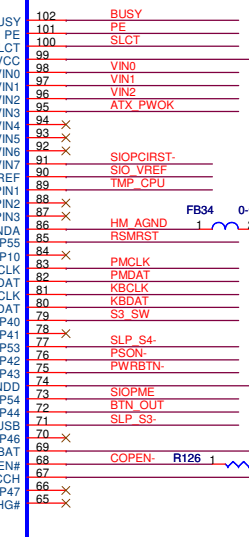
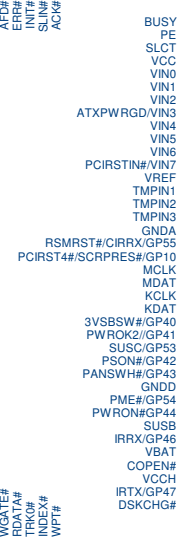
RSTSW-
IDE_RST-
PWOK
PCIE_RST-
SIOPCIRST-
LDRO-

SERIRQ
LFRAME
LAD0
LAD1
LAD2
LAD3
SIOKBRST
SIOKBRST
GA20
PCICLK_SIO
SIO_CLK

Power On Strap.

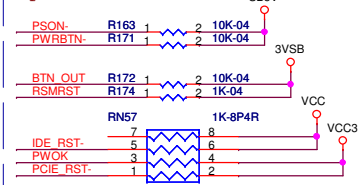


IT8713F-S/JX-L

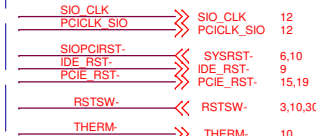
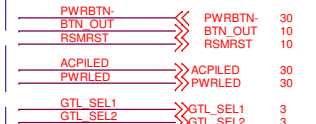


SIRO
LFRAME
LAD0
LAD1
LAD2
LAD3
SIOKBRST
SIOKBRST
GA20
PCICLK_SIO
SIO_CLK

Open Drain



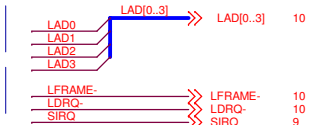
ACPI & Others



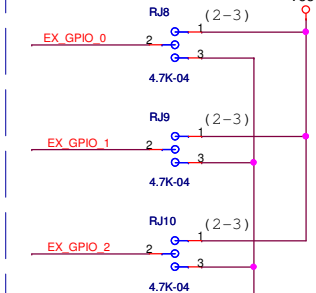
SMART FAN



LPC



GPIO

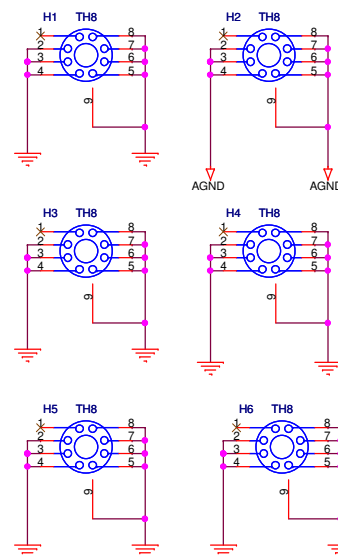
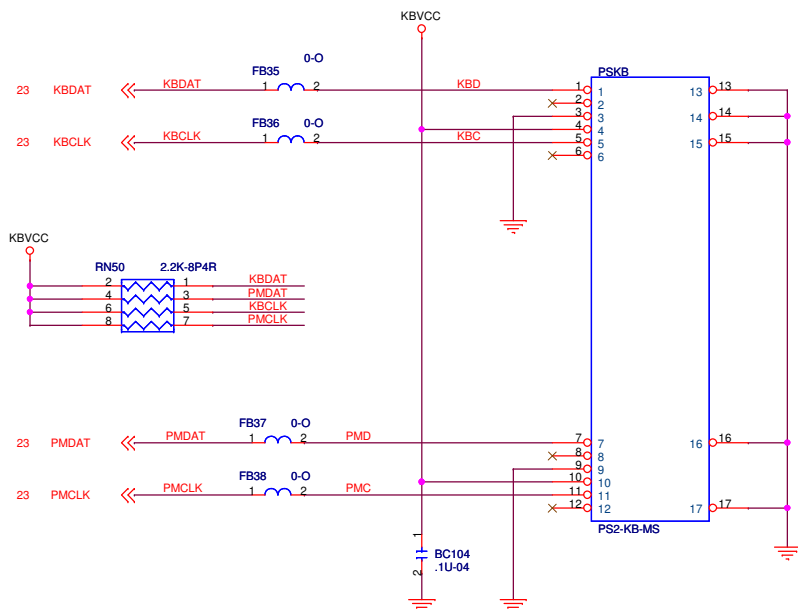
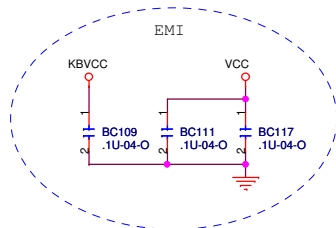


EX_GPIO_0 = 0 -> LPT HW Enable
EX_GPIO_0 = 1 -> LPT HW Disable

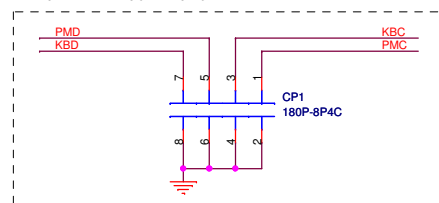


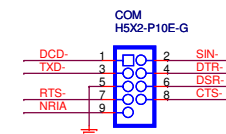
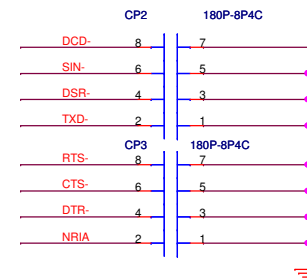
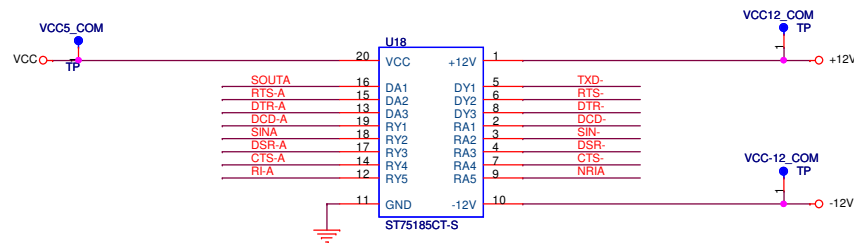
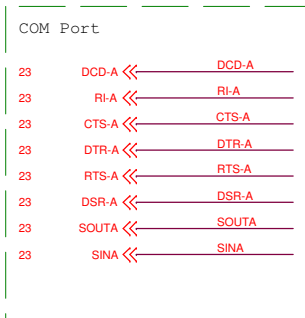
Elitegroup Computer Systems

Title: 23-Super I / O (I T8713)
 Size: Custom
 Document Number: G41T-M7
 Date: Friday, May 15, 2009
 Sheet: 23 of 30
 Rev: 1.0



PLACE NEAR CONNECTOR

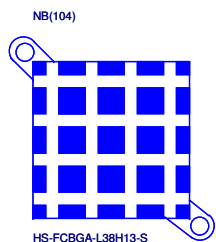




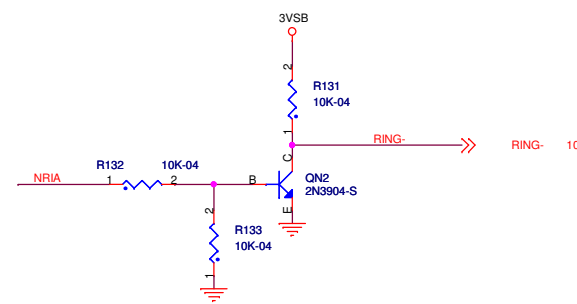
For 104



For 103



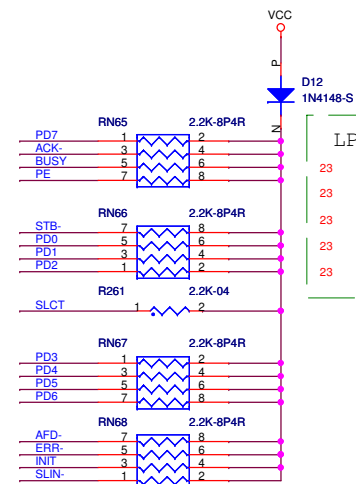
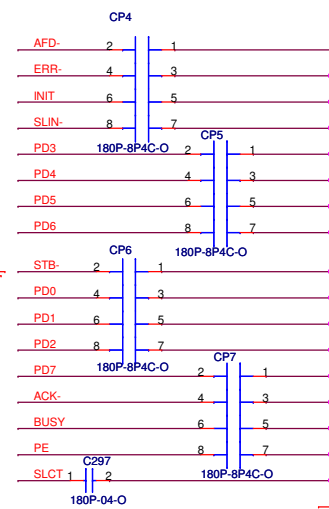
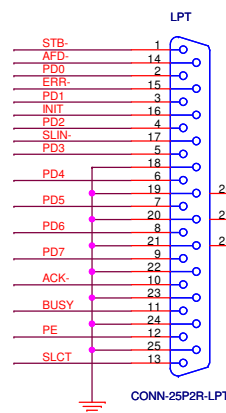
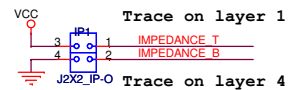
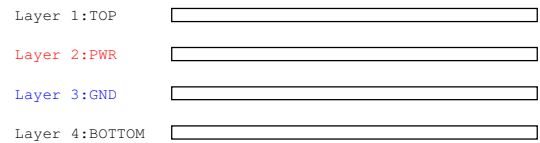
If need 25mm height :
20-120-010937 or 20-120-011420

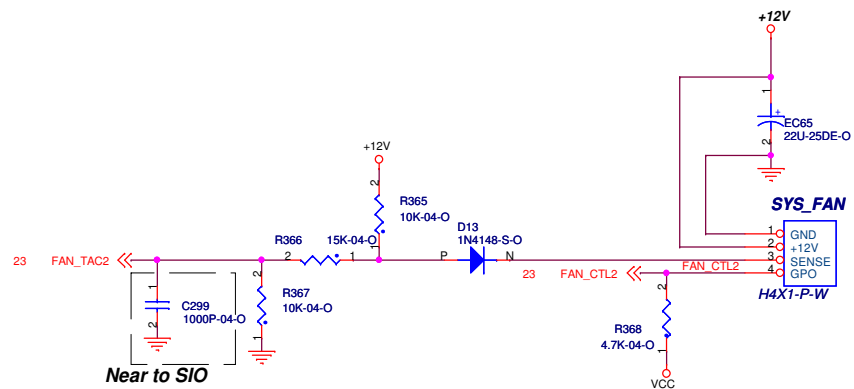
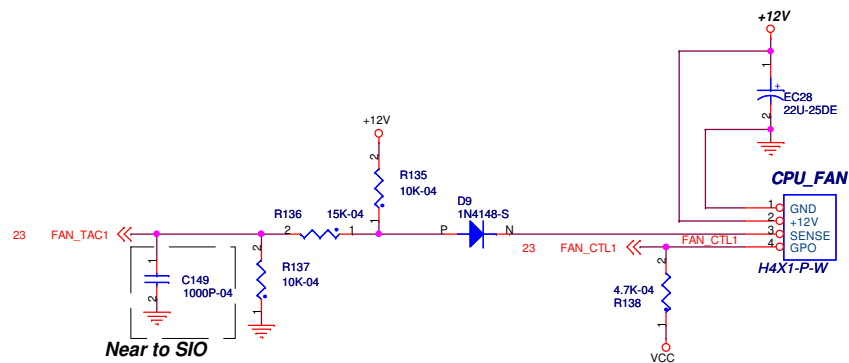


PCB Impedance control

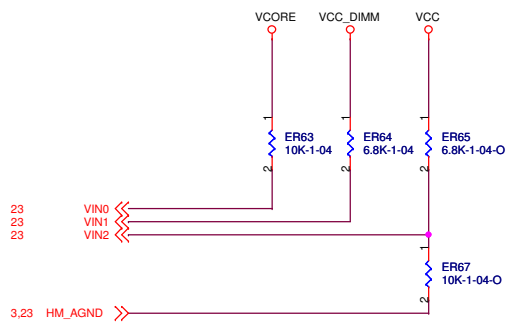
Impedance (ohm)	Trace Width (mil)	Trace Length (S/W/S)	Pre-preg
60	5	(20/5/20)	2116
50	4	(50/4/50)	1080
42	6	(50/6/50)	1080

1)Circuit type 1



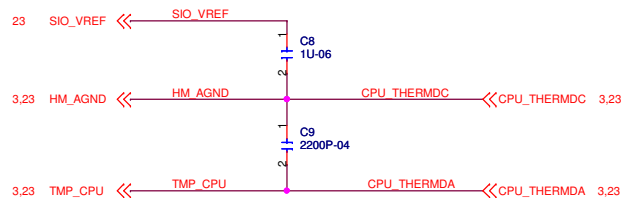


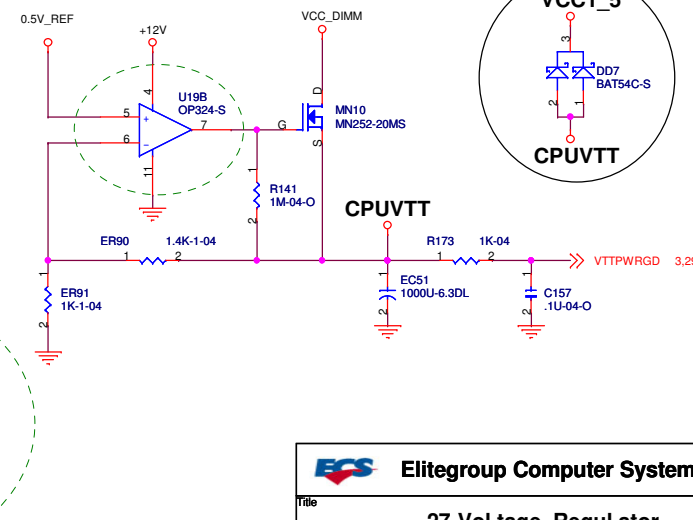
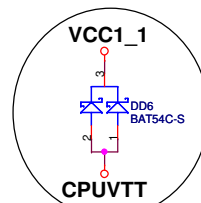
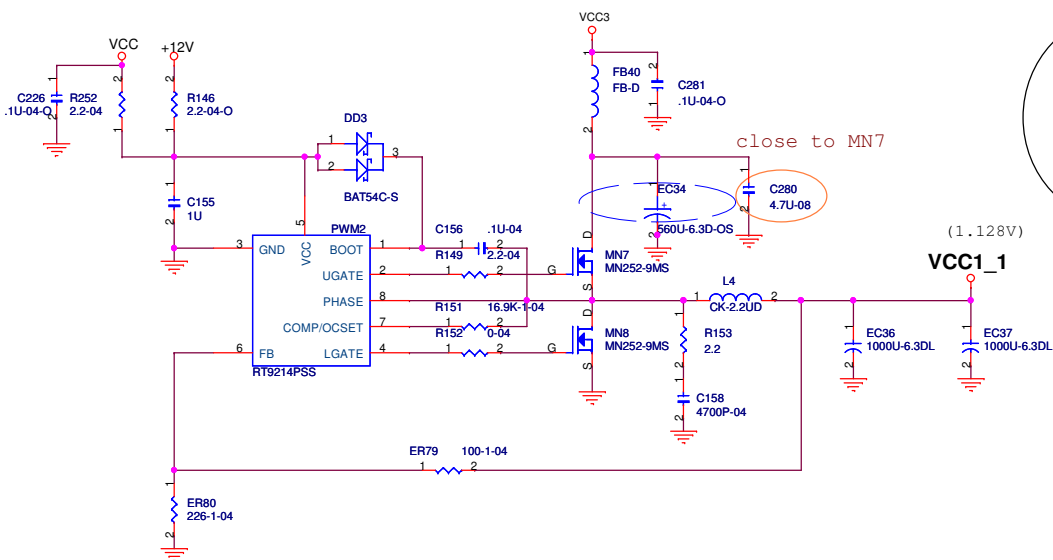
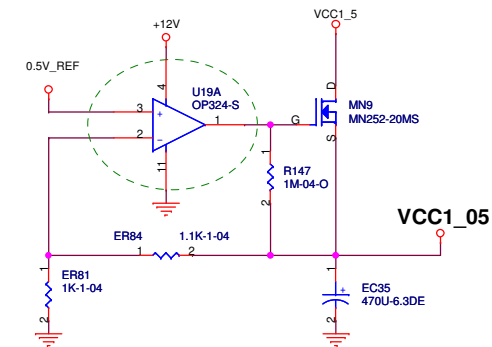
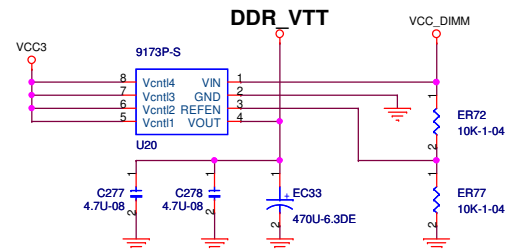
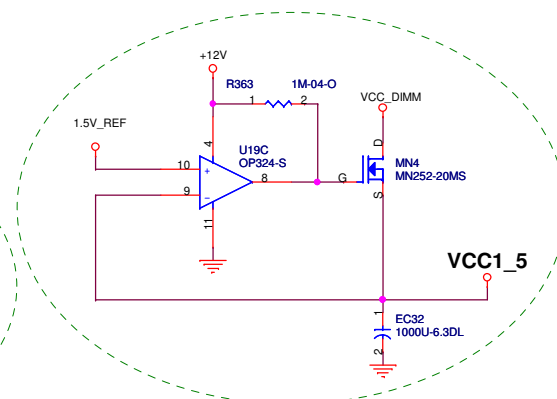
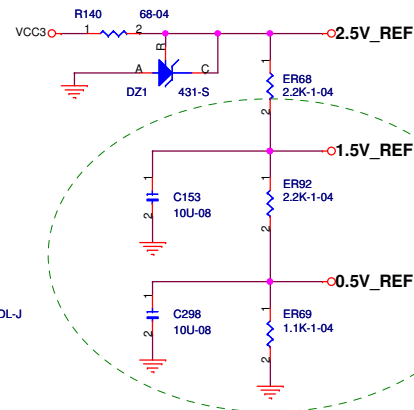
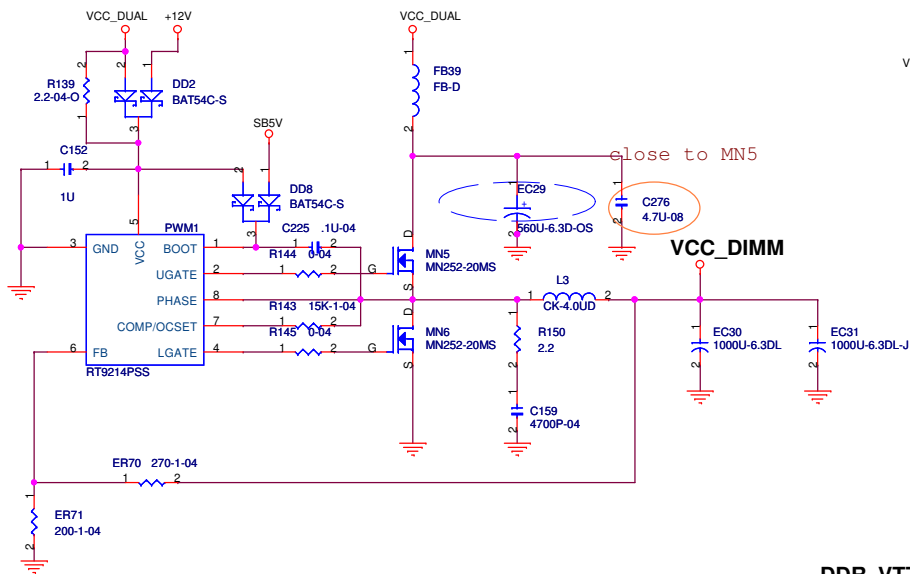
Voltage Monitor

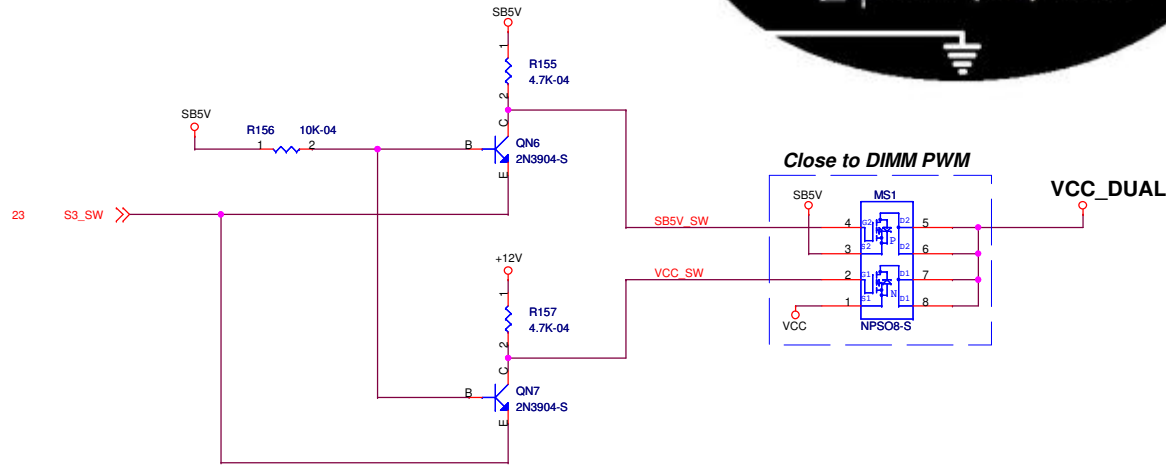
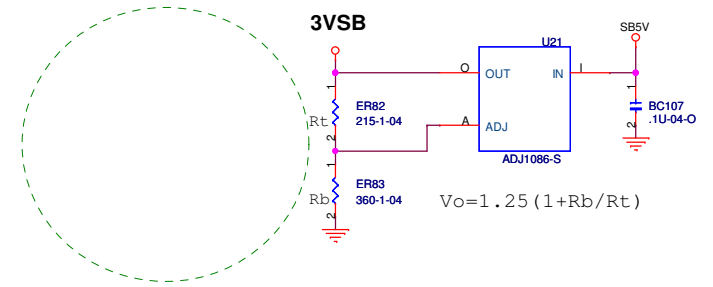
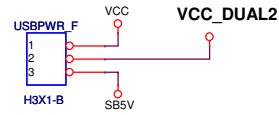
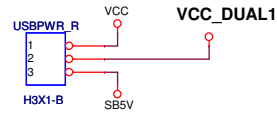


Temperature Monitor

Choosing method of measuring temperature by either thermistor or diode







Memory Power Output Control

	<i>VCC_DUAL</i>	<i>ATX_PWOK</i>	<i>SLP_S4-</i>	<i>SLP_S3-</i>	<i>S3_SW</i>
<i>S0</i>	<i>VCC</i>	<i>1</i>	<i>1</i>	<i>1</i>	<i>1</i>
<i>S1</i>	<i>VCC</i>	<i>1</i>	<i>1</i>	<i>1</i>	<i>1</i>
<i>S3</i>	<i>SB5V</i>	<i>0</i>	<i>1</i>	<i>0</i>	<i>0</i>
<i>S4</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>1</i>
<i>S5</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>0</i>	<i>1</i>

Pin connection diagram for the CPU module:

Left Header Pin	Right Header Pin
VCC	OVCC
VCORE	OVCORE
CPUVTT	OCPUVTT
CPUVID[0..7]	CPUVID[0..7]
VCC_SENSE	VCC_SENSE
VSS_SENSE	VSS_SENSE
3.27 VTT_PWRGD	VTT_PWRGD
10,12 VCORE_PWRGD	VRM_PWRGD

