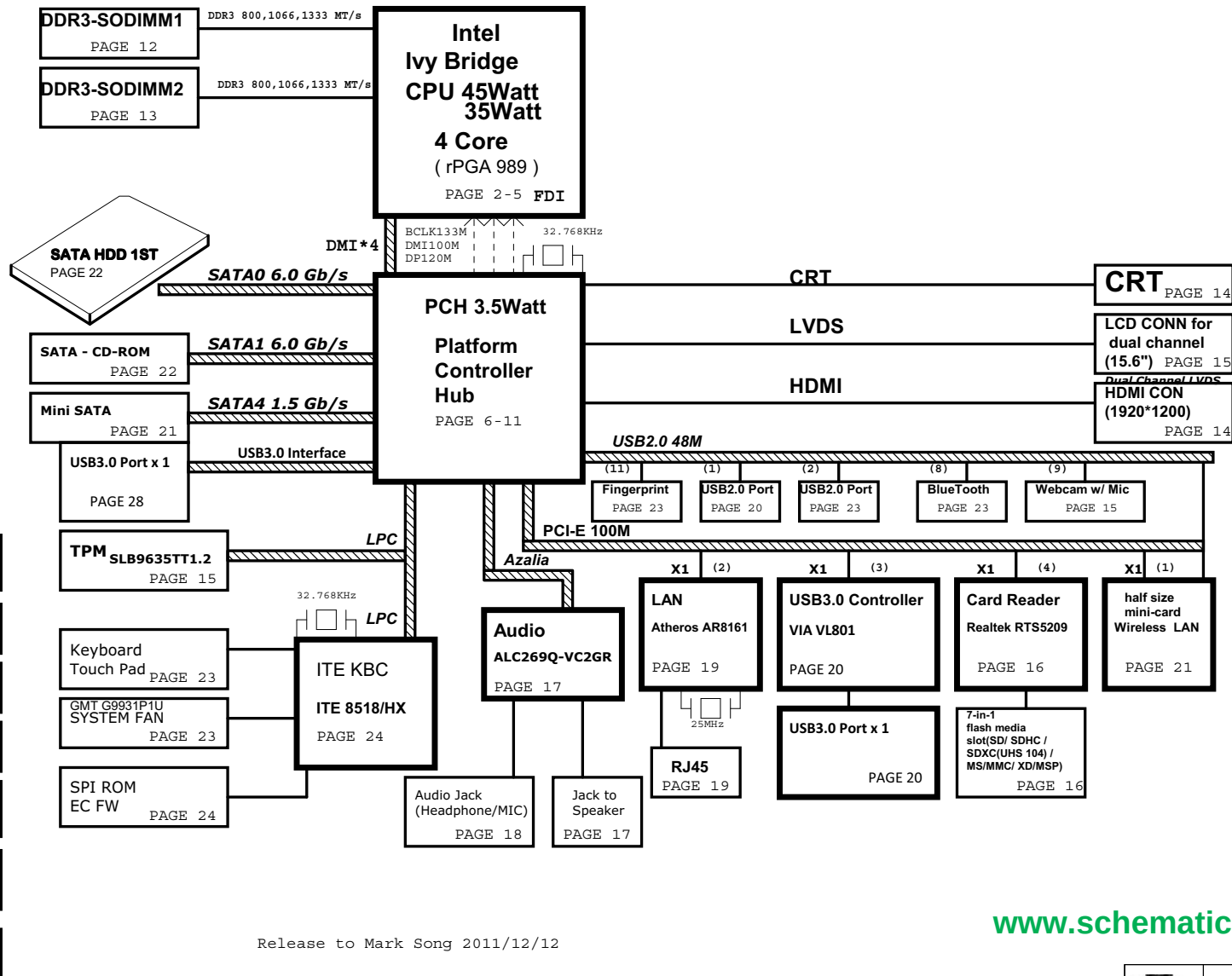


# LG2C/4C 14"/15.6" UMA BLOCK DIAGRAM

01

## PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT(Low)



Release to Mark Song 2011/12/12

[www.schematic-x.blogspot.com](http://www.schematic-x.blogspot.com)

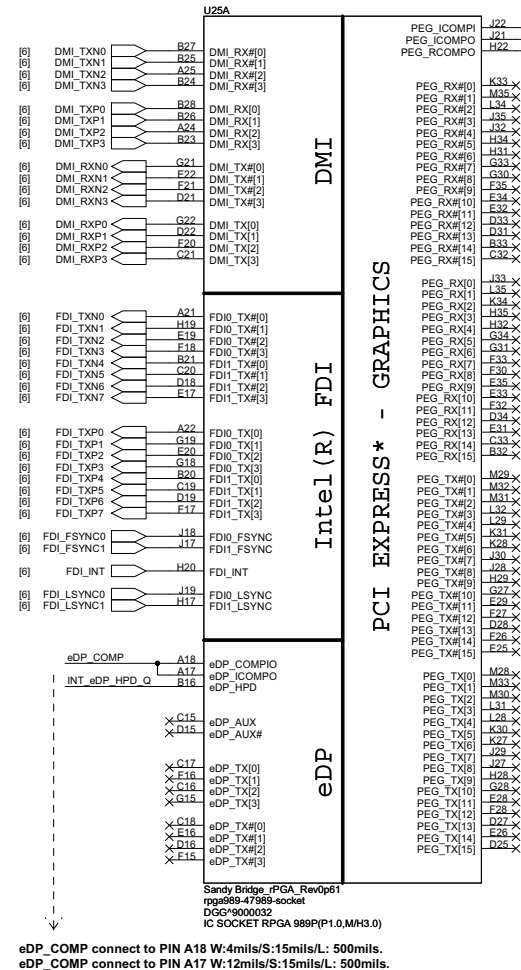


PROJECT : LGx UMA  
Quanta Computer Inc.

|                                 |                               |        |
|---------------------------------|-------------------------------|--------|
| Size Custom                     | Document Number BLOCK DIAGRAM | Rev 1A |
| Date: Monday, December 12, 2011 | Sheet 1 of 35                 |        |

## Sandy Bridge Processor (DMI, PEG, FDI)

## Sandy Bridge Processor (CLK, MISC, JTAG)



PEG\_ICOMPO J22 PEG\_COMP  
PEG\_ICOMPO J21 PEG\_COMP  
PEG\_ICOMPO J22 PEG\_COMP

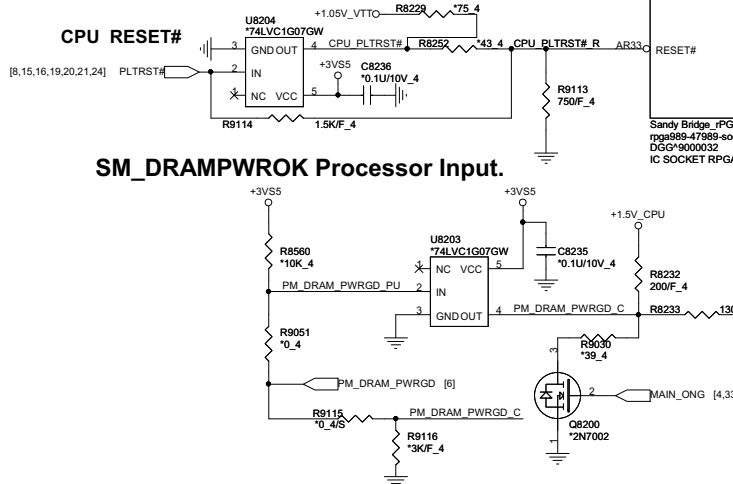
PEG\_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.  
PEG\_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

SNB\_IVB# N.A at SNB EDS #27637 0.7v1

Placement close to EC.

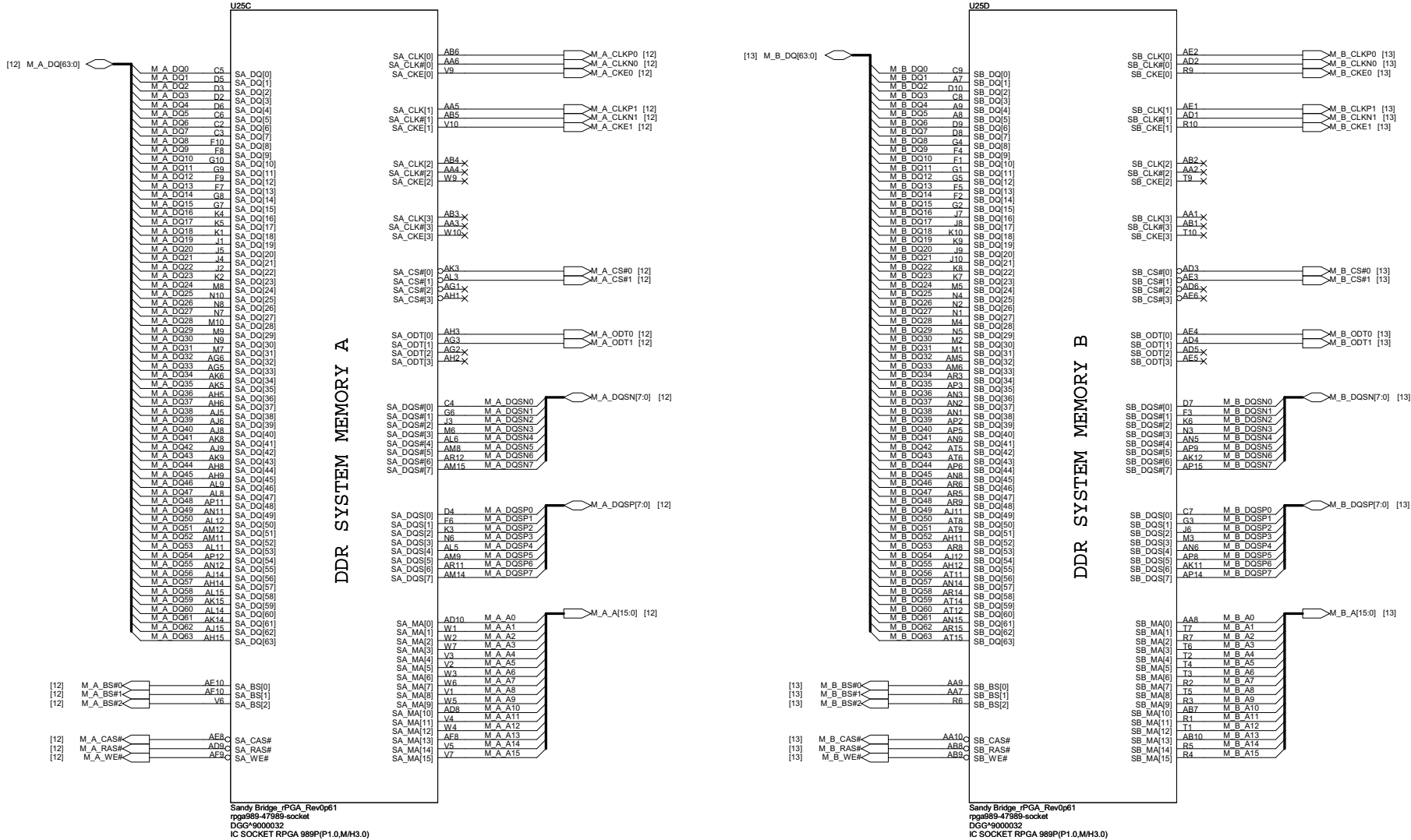
CPU RESET#

SM\_DRAMPWROK Processor Input.

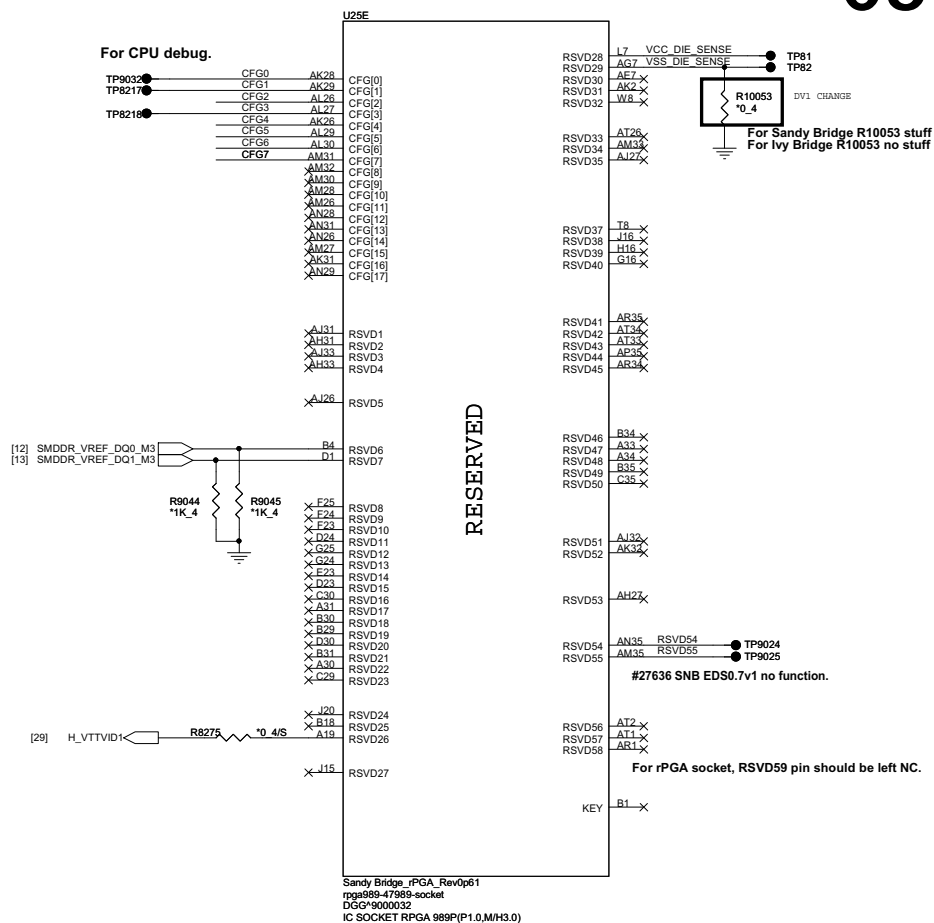


# Ivy Bridge Processor (DDR3)

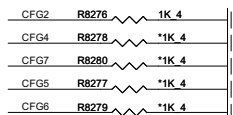
03







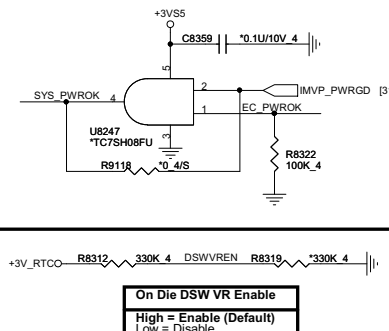
```
CFG[6:5] (PCIe Port Bifurcation Straps)
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```



|                                                                                                     |                                                         |                                  |           |
|-----------------------------------------------------------------------------------------------------|---------------------------------------------------------|----------------------------------|-----------|
| <br><b>NB5</b> | <b>PROJECT : LGx UMA</b><br><b>Quanta Computer Inc.</b> |                                  |           |
|                                                                                                     | Size Custom                                             | Document Number<br>SNB 4/4 (GND) | Rev<br>1A |
| Date: Monday, December 05, 2011                                                                     |                                                         | Sheet 5 of 35                    |           |



## System PWR\_OK(CLG)

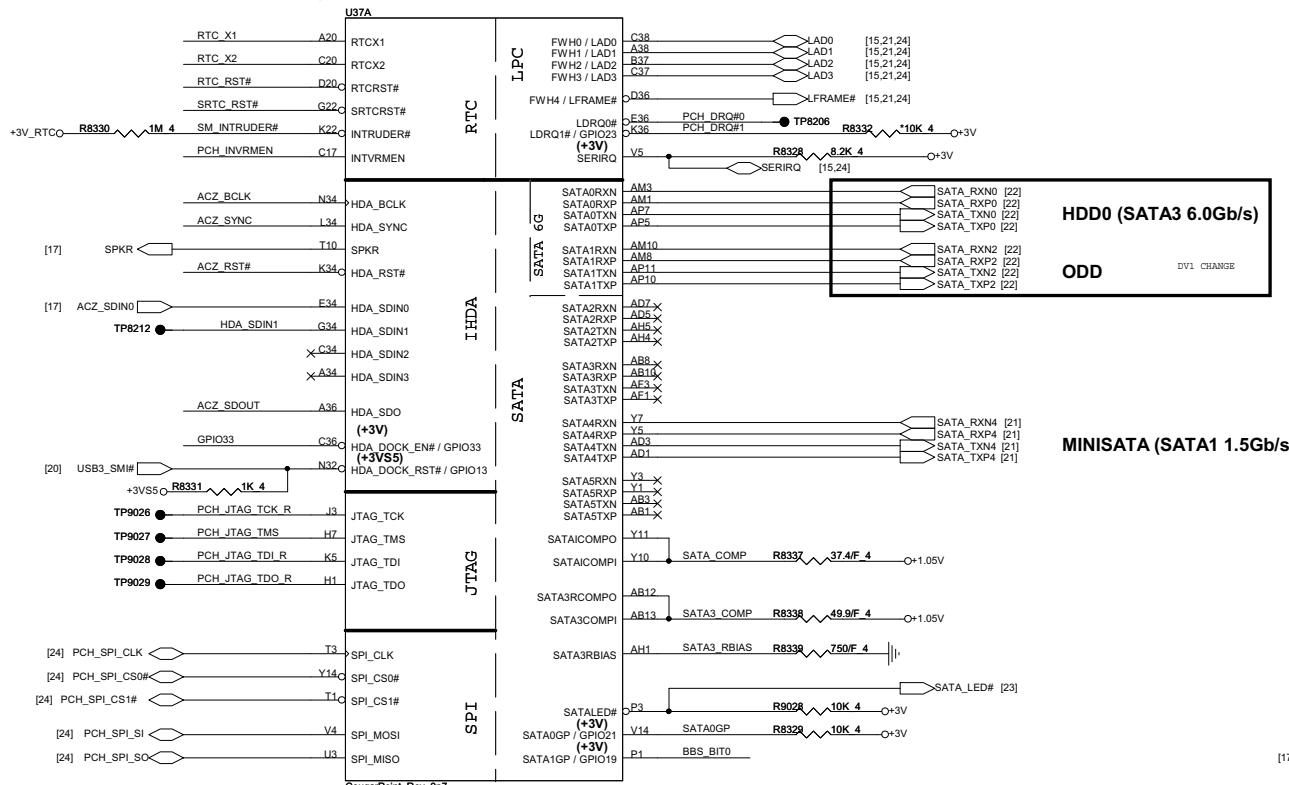


**PROJECT : LGx UMA**  
**Quanta Computer Inc.**

|        |                         |
|--------|-------------------------|
| Size   | Document Number         |
| Custom | PCH 1/6 (DMI/FDI/VIDEO) |

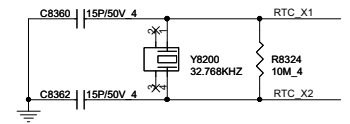
Rev  
1A

# Cougar Point (HDA,JTAG,SATA)

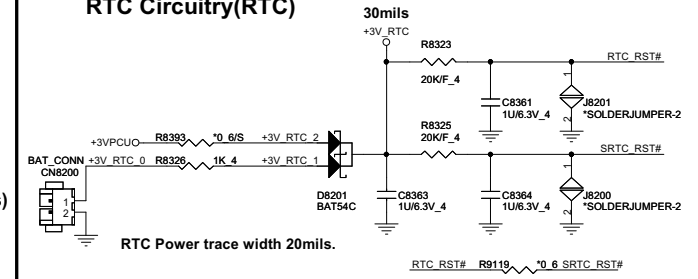


## RTC Clock 32.768KHz

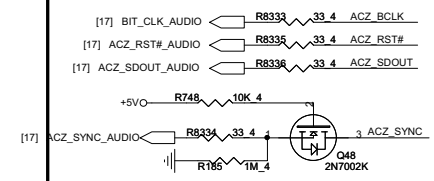
07



## RTC Circuitry(RTC)

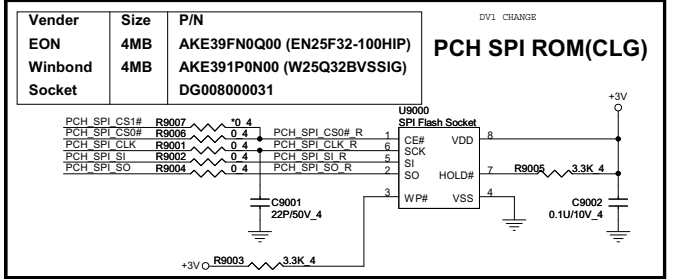


## HDA Bus(CLG)



## PCH Strap Table

| Pin Name            | Strap description                                   | Sampled                       | Configuration                                                                                                                                                                                         | Circuit                                                           |       |               |   |   |     |   |   |     |                                                                           |
|---------------------|-----------------------------------------------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|-------|---------------|---|---|-----|---|---|-----|---------------------------------------------------------------------------|
| SPKR                | Different from Calpella                             | No reboot mode setting        | PWROK                                                                                                                                                                                                 | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode |       |               |   |   |     |   |   |     |                                                                           |
| GNT3# / GPIO55      | Top-Block Swap Override                             | PWROK                         | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K)                                                                                                                                           |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| INTVRMEN            | Integrated 1.05V VRM enable                         | ALWAYS                        | Should be always pull-up                                                                                                                                                                              |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security Only for Interposer       | PWROK                         | 0 = Override<br>1 = Default (weak pull-up 20K)                                                                                                                                                        |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| GNT1# / GPIO51      | Boot BIOS Selection 1 [bit-1]                       | PWROK                         | <table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table> | GNT1#                                                             | GNT0# | Boot Location | 1 | 0 | SPI | 0 | 0 | LPC | [Need external pull-down for LPC BIOS]<br>Default weak pull-up on GNT0/1# |
| GNT1#               | GNT0#                                               | Boot Location                 |                                                                                                                                                                                                       |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| 1                   | 0                                                   | SPI                           |                                                                                                                                                                                                       |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| 0                   | 0                                                   | LPC                           |                                                                                                                                                                                                       |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| GPIO19              | Different from Calpella                             | Boot BIOS Selection 0 [bit-0] | PWROK                                                                                                                                                                                                 |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| GNT2# / GPIO53      | ESI strap (Server only)                             | PWROK                         | Should not be pull-down (weak pull-up 20K)                                                                                                                                                            | USE GPIO PIN                                                      |       |               |   |   |     |   |   |     |                                                                           |
| NV_ALE              | Intel Anti-Theft HDD protection Only for Interposer | PWROK                         | 0 = Disable (Internal pull-down 20kohm)                                                                                                                                                               |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| NV_CLE              | DMI Termination voltage                             | PWROK                         | weak pull-down 20kohm                                                                                                                                                                                 |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| HDA_SYNC            | On-Die PLL VR Voltage Select                        | RSMRST                        | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V                                                                                                                                           |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| HDA_SDO             | Flash Descriptor Security                           | PWROK                         | 0 = Override<br>1 = Default (weak pull-up 20K)                                                                                                                                                        |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| GPIO8               | Integrated Clock Chip Enable                        | RSMRST#                       | Should be pull-down (weak pull-up 20K)                                                                                                                                                                |                                                                   |       |               |   |   |     |   |   |     |                                                                           |
| GPIO28              | Different from Calpella                             | On-die PLL Voltage Regulator  | RSMRST#                                                                                                                                                                                               | 0 = Disable<br>1 = Enable (Default)                               |       |               |   |   |     |   |   |     |                                                                           |
| SPI_MOSI            | iTPM function Disable                               | APWROK                        | 0 = Default (weak pull-down 20K)<br>1 = Enable                                                                                                                                                        |                                                                   |       |               |   |   |     |   |   |     |                                                                           |

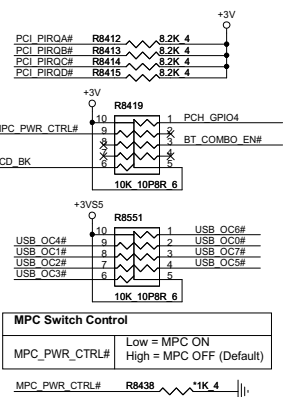


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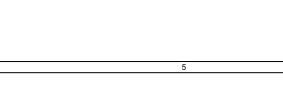
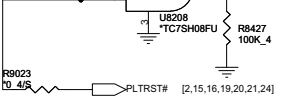
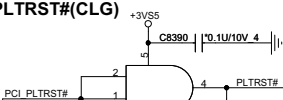
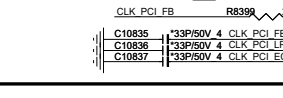
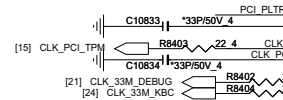
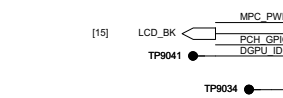
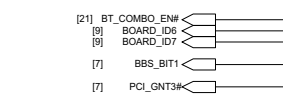
|                                 |                                        |        |
|---------------------------------|----------------------------------------|--------|
| Size Custom                     | Document Number PCH 2/6 (SATA/HDA/SPI) | Rev 1A |
| Date: Monday, December 05, 2011 | Sheet 7 of 35                          |        |

Cougar Point-M (PCI,USB,NVRAM)

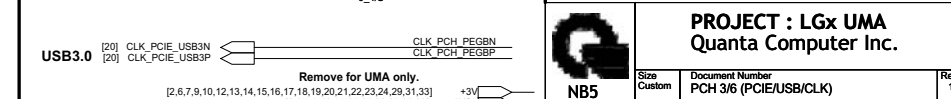
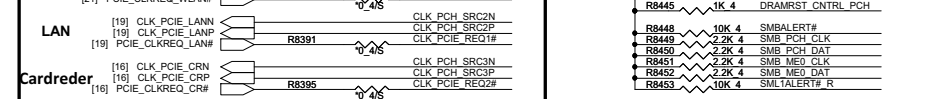
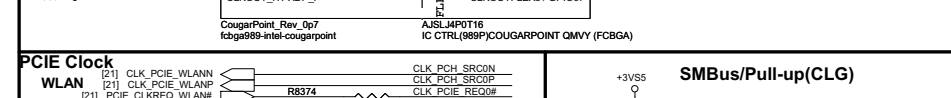
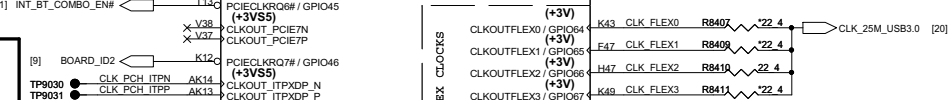
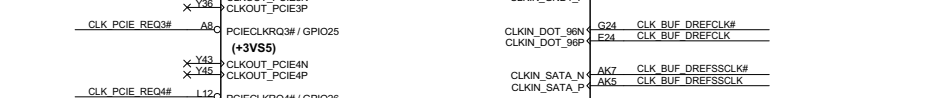
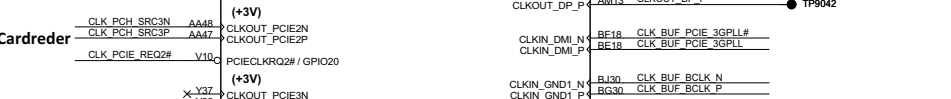
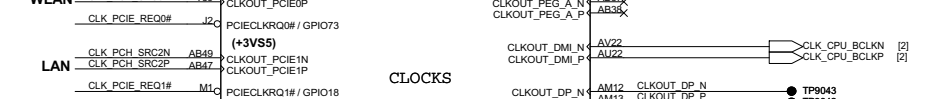
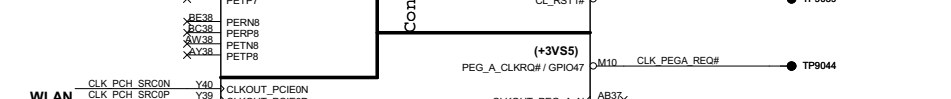
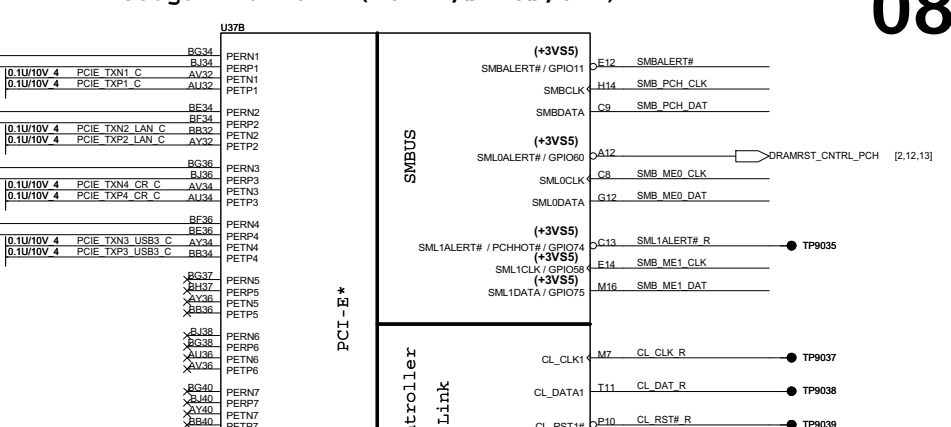
PCI/USBOC# Pull-up(CLG)



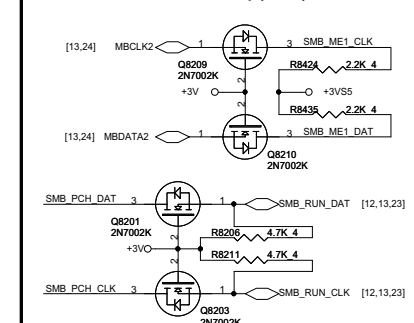
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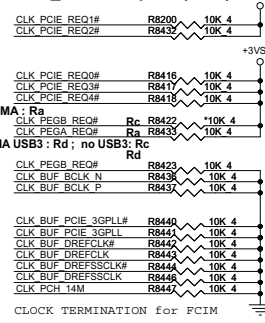
Cougar Point-M (PCI-E, SMBUS, CLK)



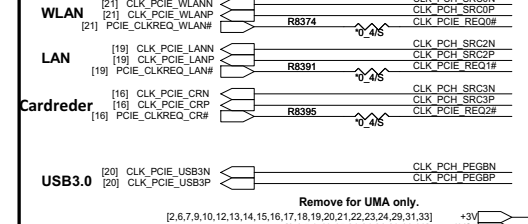
## SMBus/Pull-up(CLG)



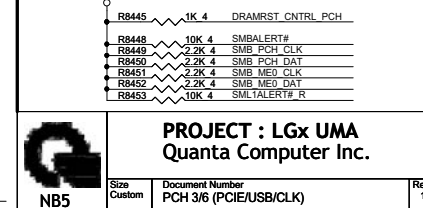
### CLK\_REQ/Strap Pin(CLG)



## PCIE Clock

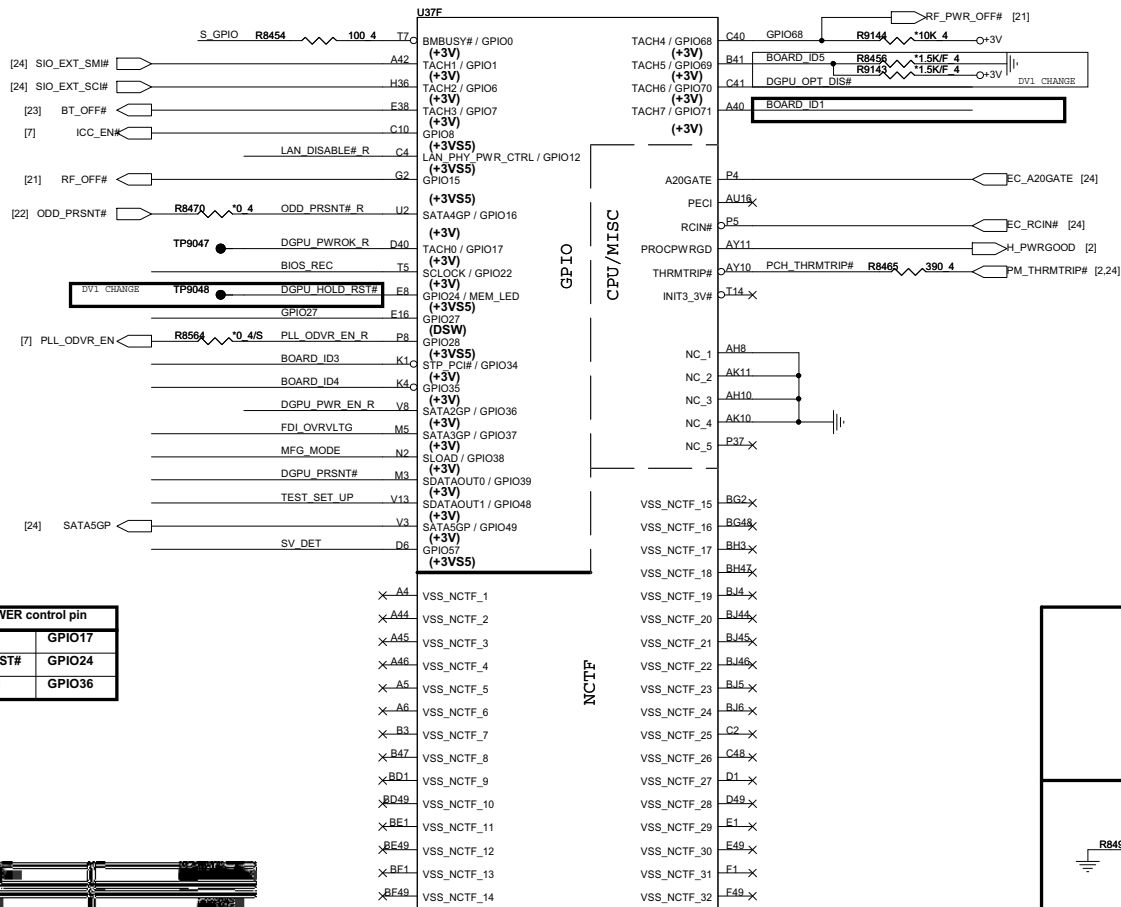


### SMBus/Pull-up(CLG)





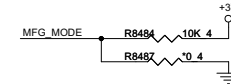
## Cougar Point (GPIO,VSS\_NCTF,RSVD)



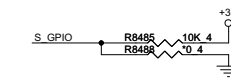
|             | Ra    | Rb    |
|-------------|-------|-------|
| UMA/Muxless | NC    | Stuff |
| DIS         | Stuff | NC    |

DGPU OPT DIS#:  
High : Muxless/UMA.  
Low : Discrete.

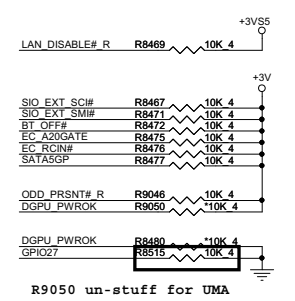
## MFG-TEST



## SGPIO



## GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer  
Security (TLS) cipher suite  
Low = Disable (Default)  
High = Enable

BIOS RECOVERY High = Disable (Default)  
Low = Enable

SV\_SET\_UP  
High = Strong (Default)

TEST DETECT  
Low = Default

DMI TERMINATION VOLTAGE OVERRIDE  
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE  
LOW - Tx, Rx terminated to same voltage

## GFX Present

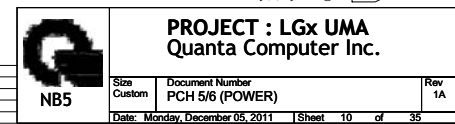
|       | DIS/Muxless | UMA |
|-------|-------------|-----|
| Stuff | Ra          | Rb  |
| NC    | Rb          | Ra  |

[2,6,7,8,10,12,13,14,15,16,17,18,19,20,21,22,23,24,29,31,33] +3V

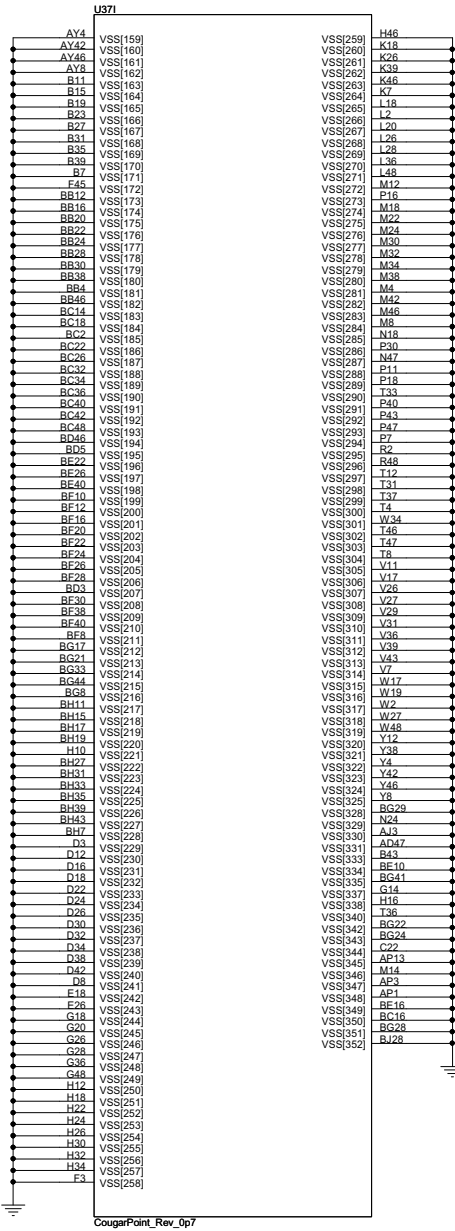


**PROJECT : LGx UMA**  
**Quanta Computer Inc.**

Size Custom Document Number PCH 4/6 (GPIO/MISC) Rev 1A  
Date: Monday, December 05, 2011 Sheet 9 of 35

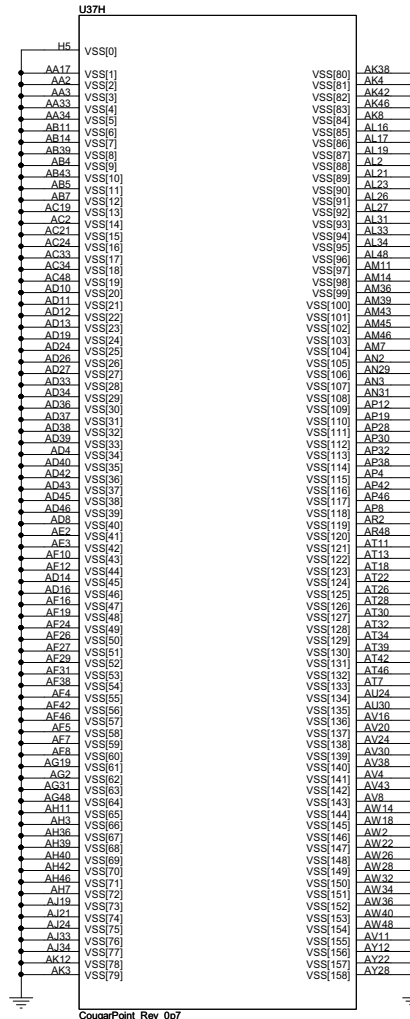


IBEX PEAK-M (GND)



CougarPoint\_Rev\_0p7

IBEX PEAK-M (GND)

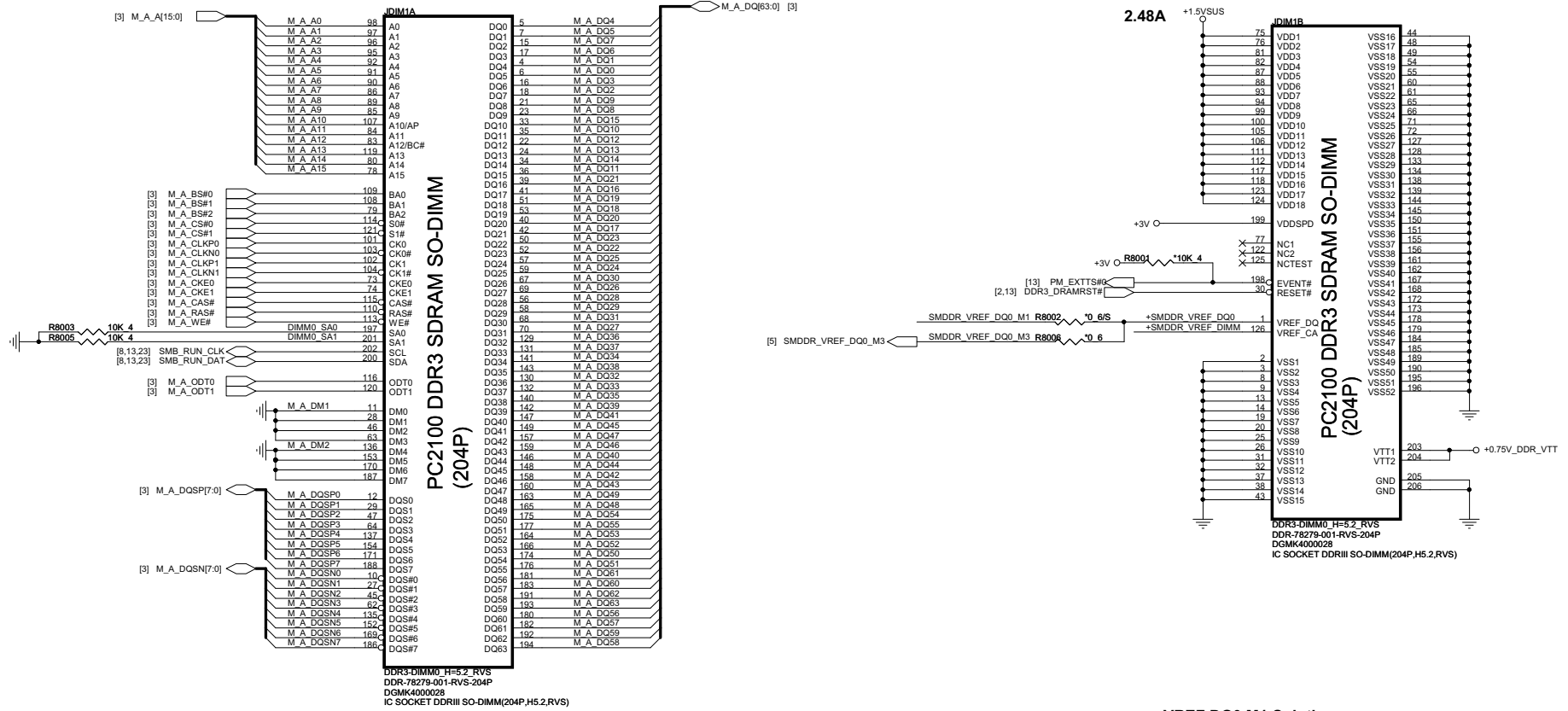


CougarPoint\_Rev\_0p7

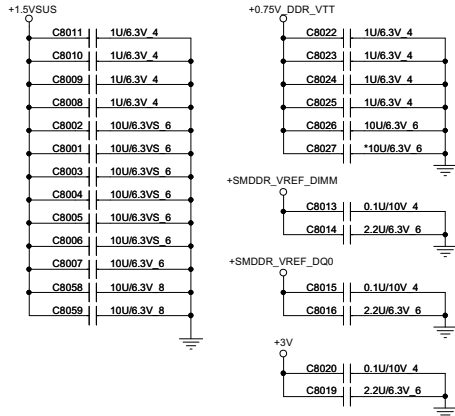


PROJECT : LGx UMA  
Quanta Computer Inc.

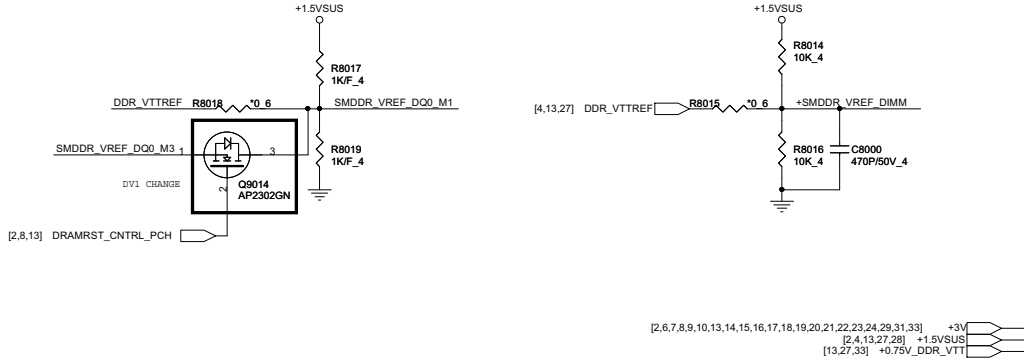
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| Date: Thursday, December 01, 2011 | Sheet 11 of 35                   |           |

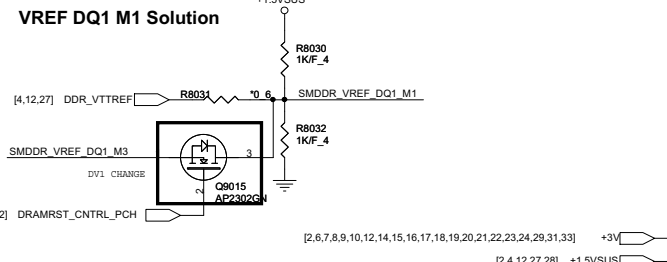
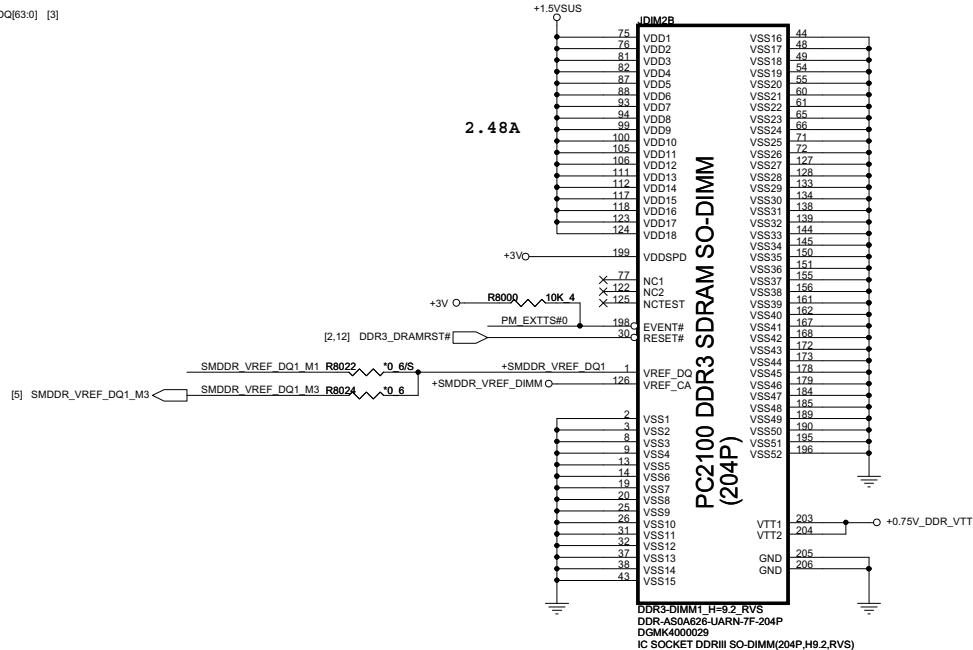


Place these Caps near So-Dimm0.

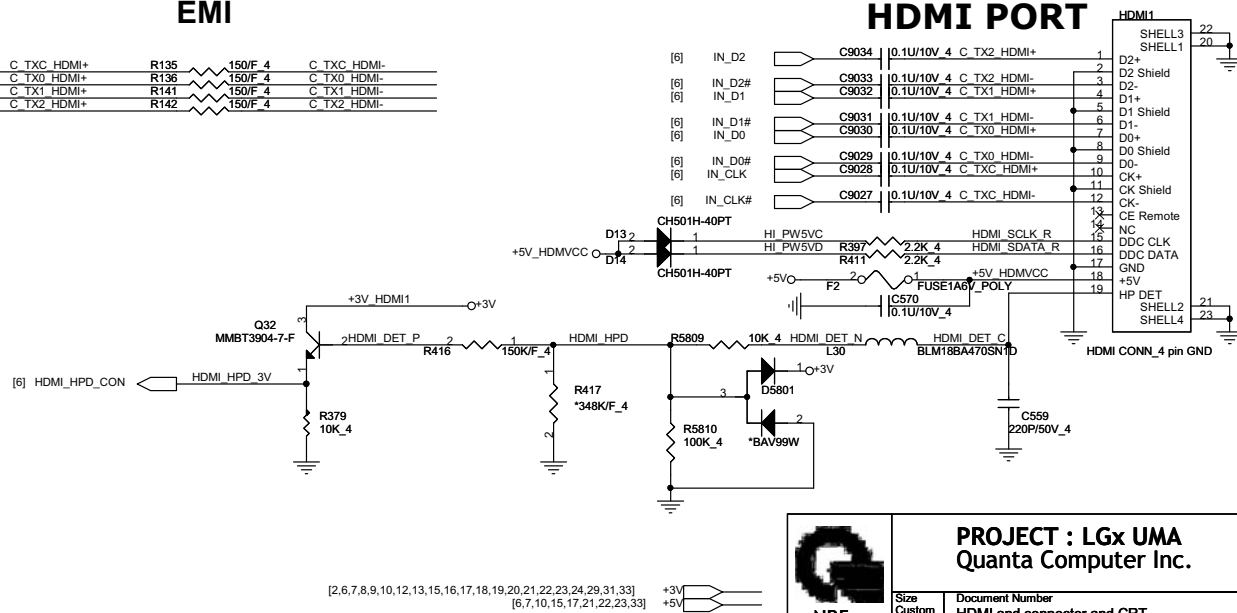


VREF DQ0 M1 Solution



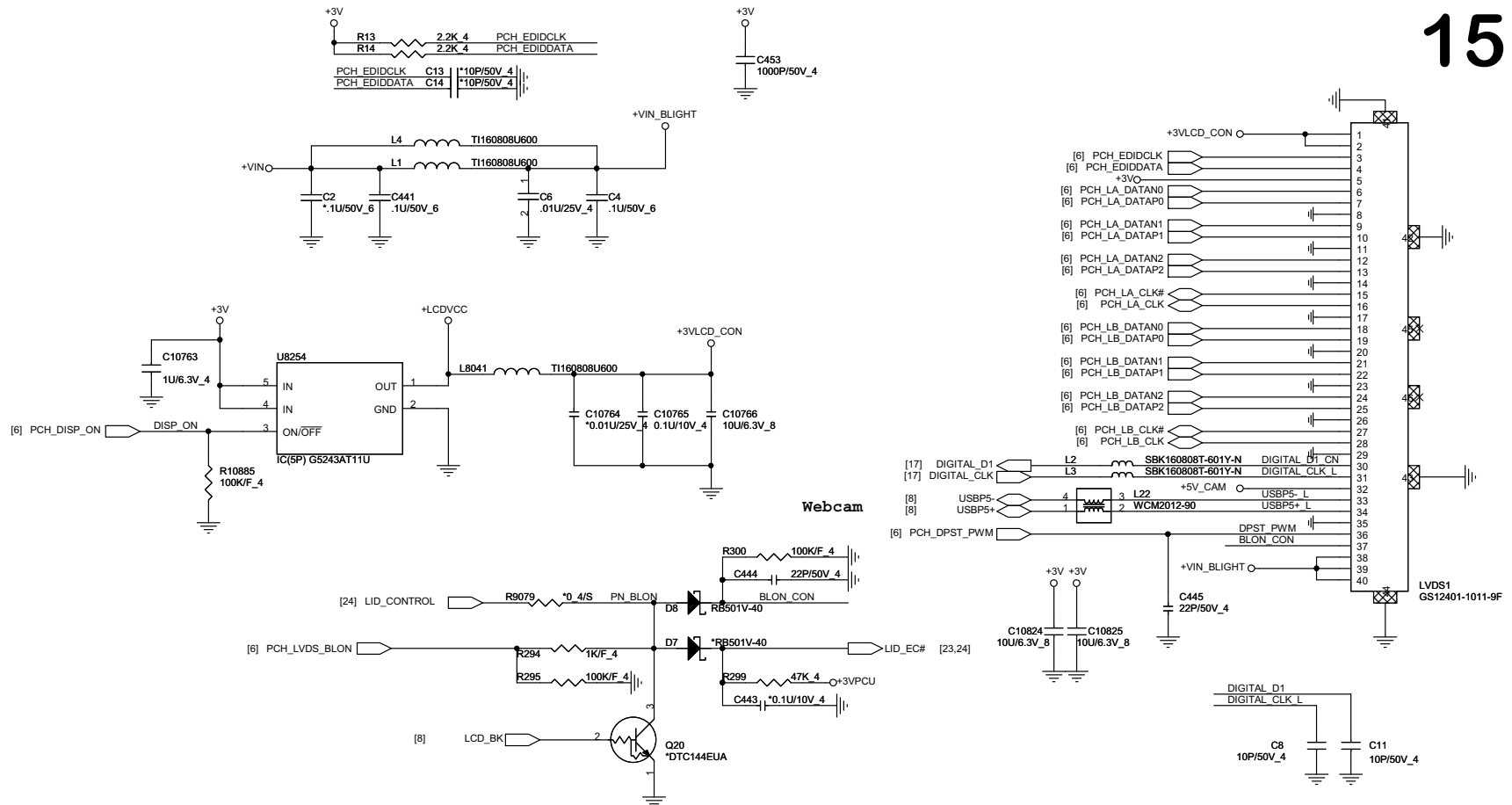
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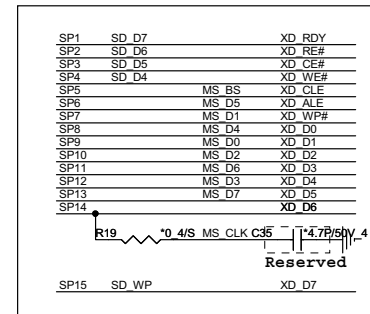
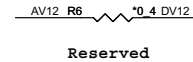
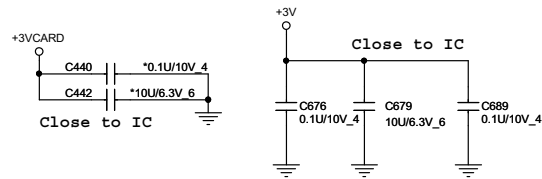
|                                 |                                          |     |
|---------------------------------|------------------------------------------|-----|
| Size Custom                     | Document Number<br>DDR3 DIMM1-RVS (9.2H) | Rev |
| Date: Monday, December 05, 2011 | Sheet 13 of 35                           |     |



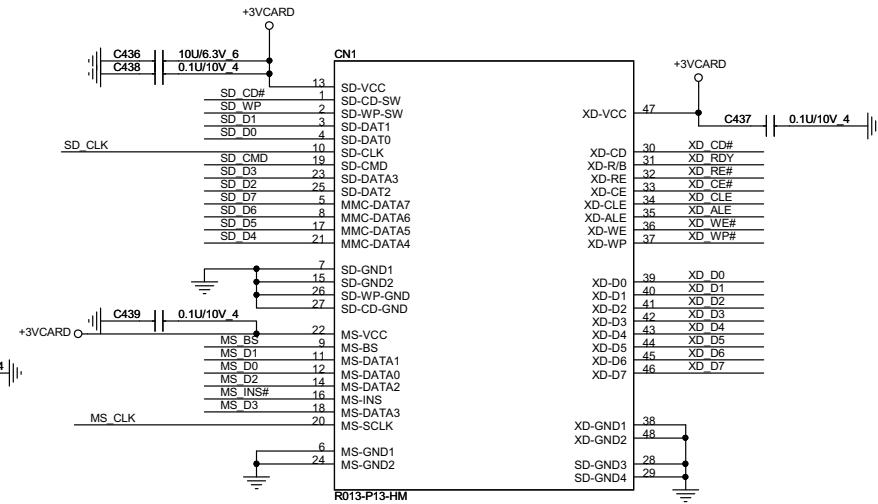
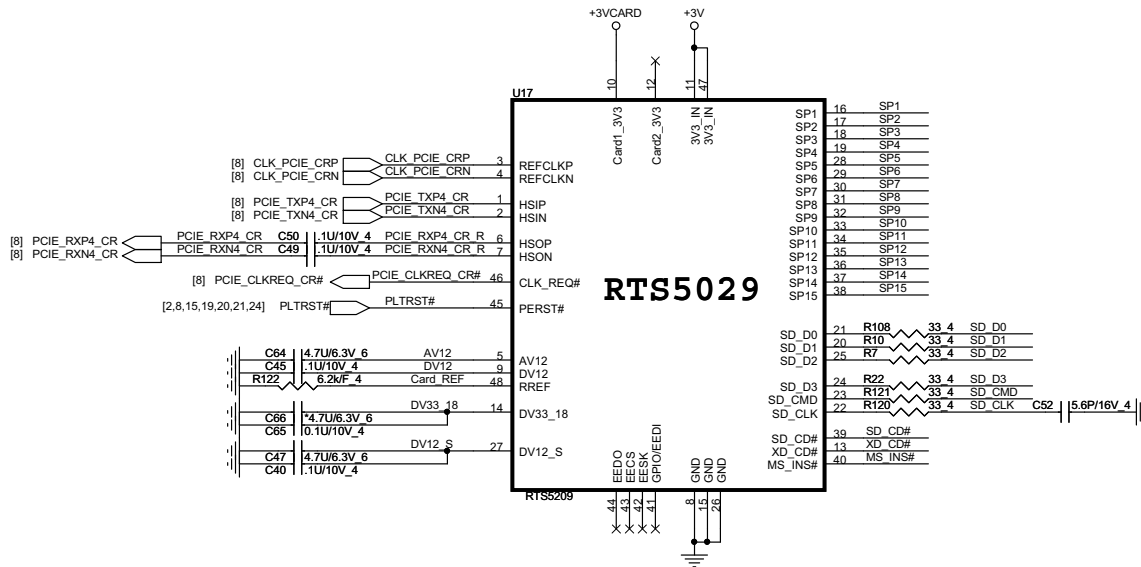
**PROJECT : LGx UMA**  
**Quanta Computer Inc.**

|                                 |                                               |           |
|---------------------------------|-----------------------------------------------|-----------|
| Size<br>Custom                  | Document Number<br>HDMI and connector and CRT | Rev<br>1A |
| Date: Monday, December 05, 2011 | Sheet 14 of 35                                |           |

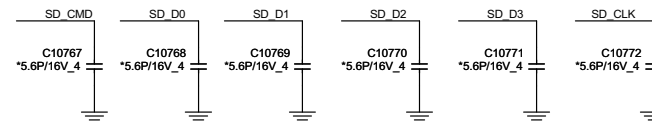




**7-in-1  
flash media  
slot(SD / SDHC / SDXC(UHS 104) / MS/MMC/ XD/ MSP)**



EMI Solution  
Please help to close to connector



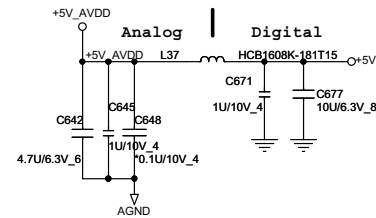
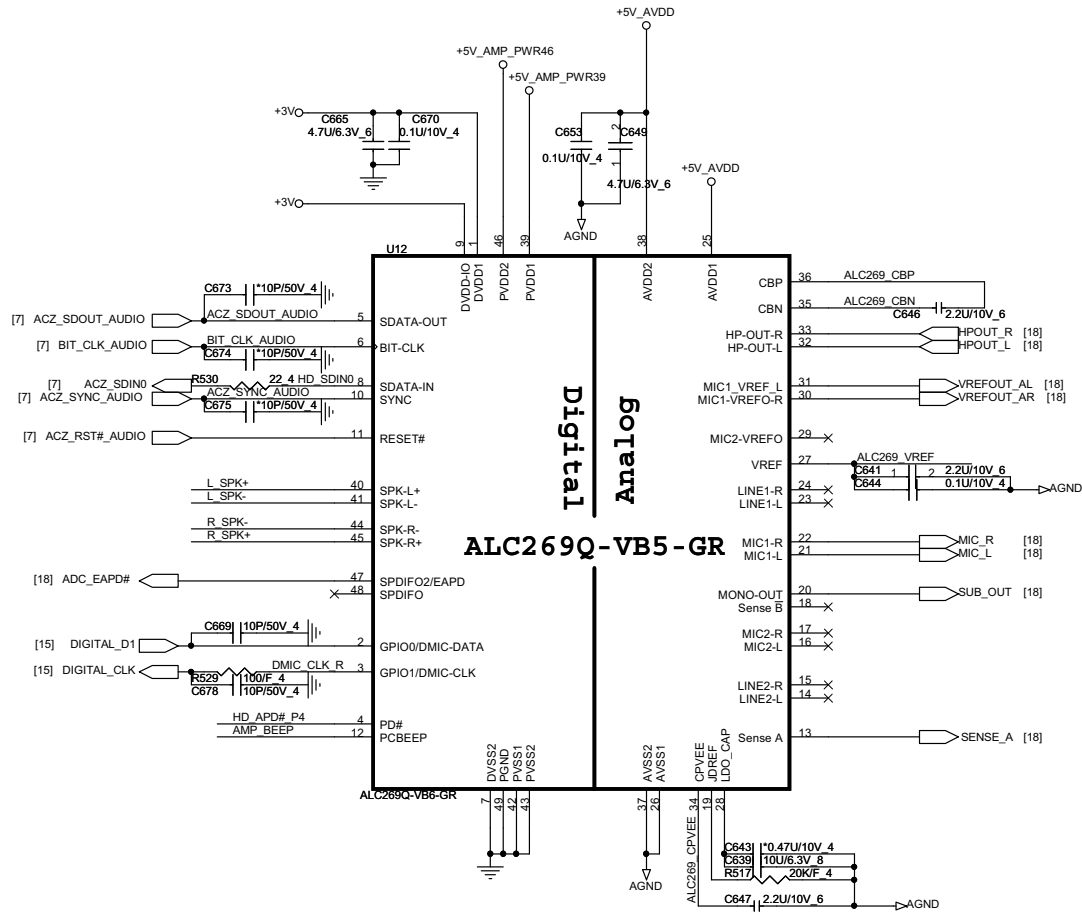
[2,6,7,8,9,10,12,13,14,15,17,18,19,20,21,22,23,24,29,31,33]

+3V

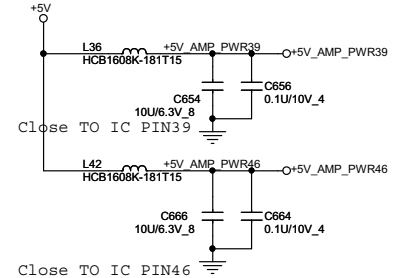
**PROJECT : LGx UMA  
Quanta Computer Inc.**

|                                                  |                                          |           |
|--------------------------------------------------|------------------------------------------|-----------|
| Size<br>Custom                                   | Document Number<br>Card reader (RTS5029) | Rev<br>1A |
| Date: Monday, December 05, 2011   Sheet 16 of 35 |                                          |           |

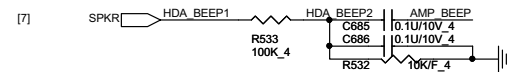
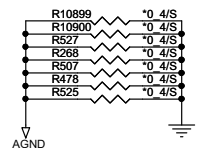
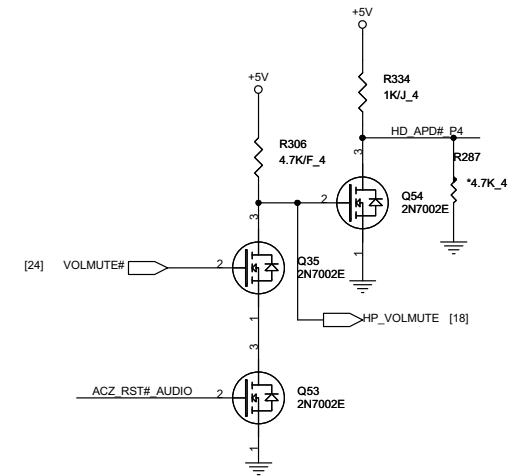
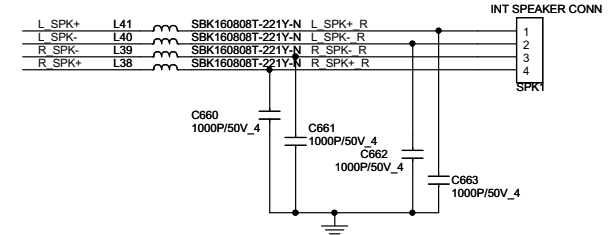




Close TO IC PIN25

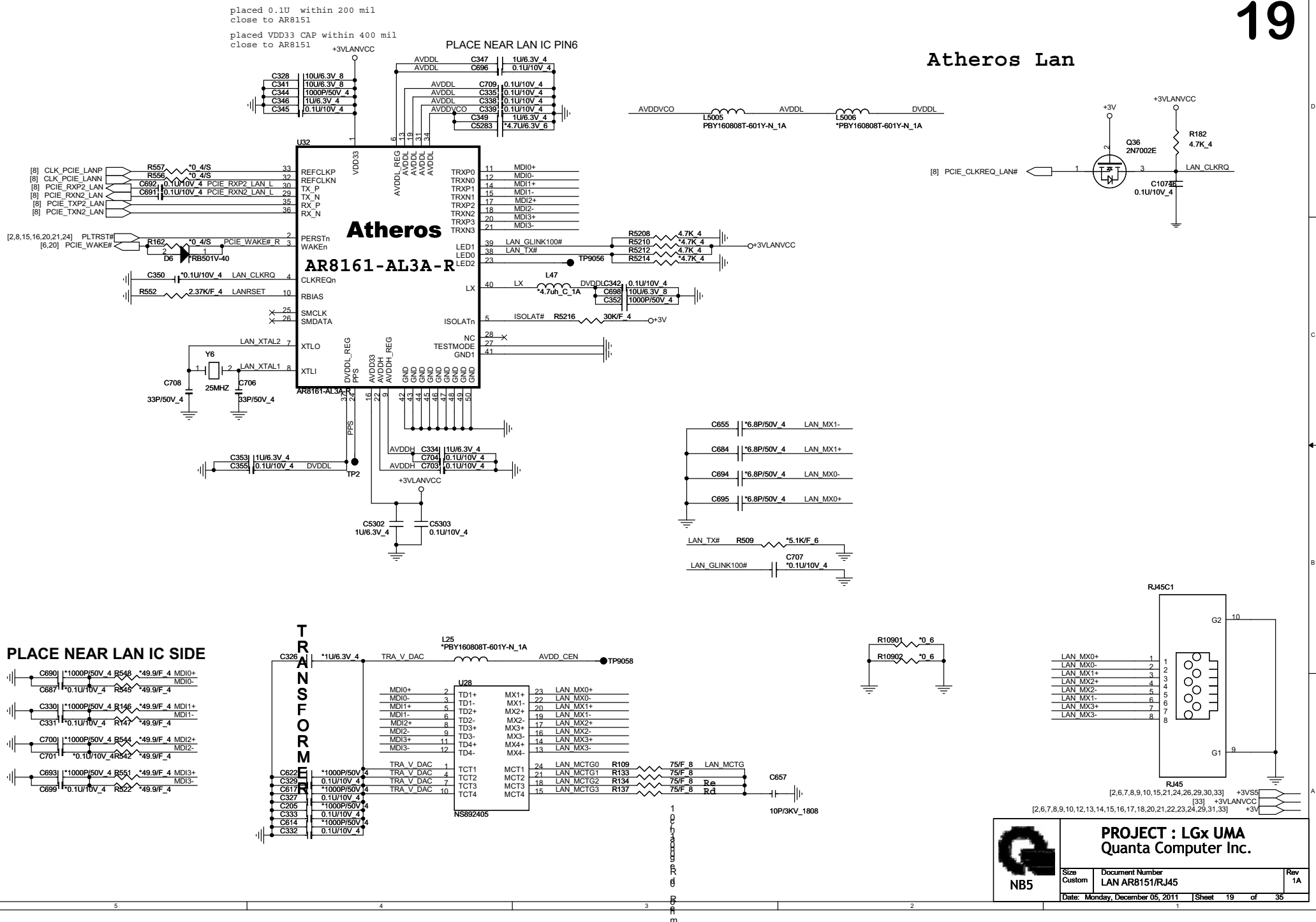


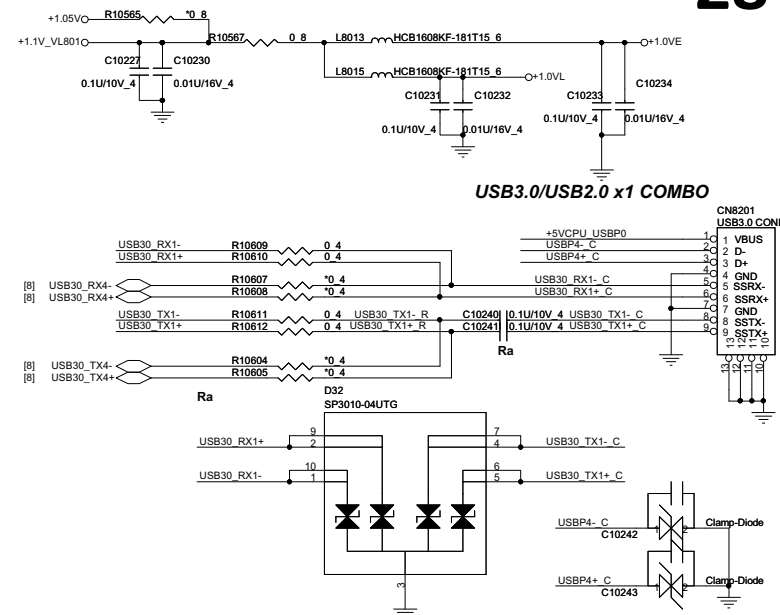
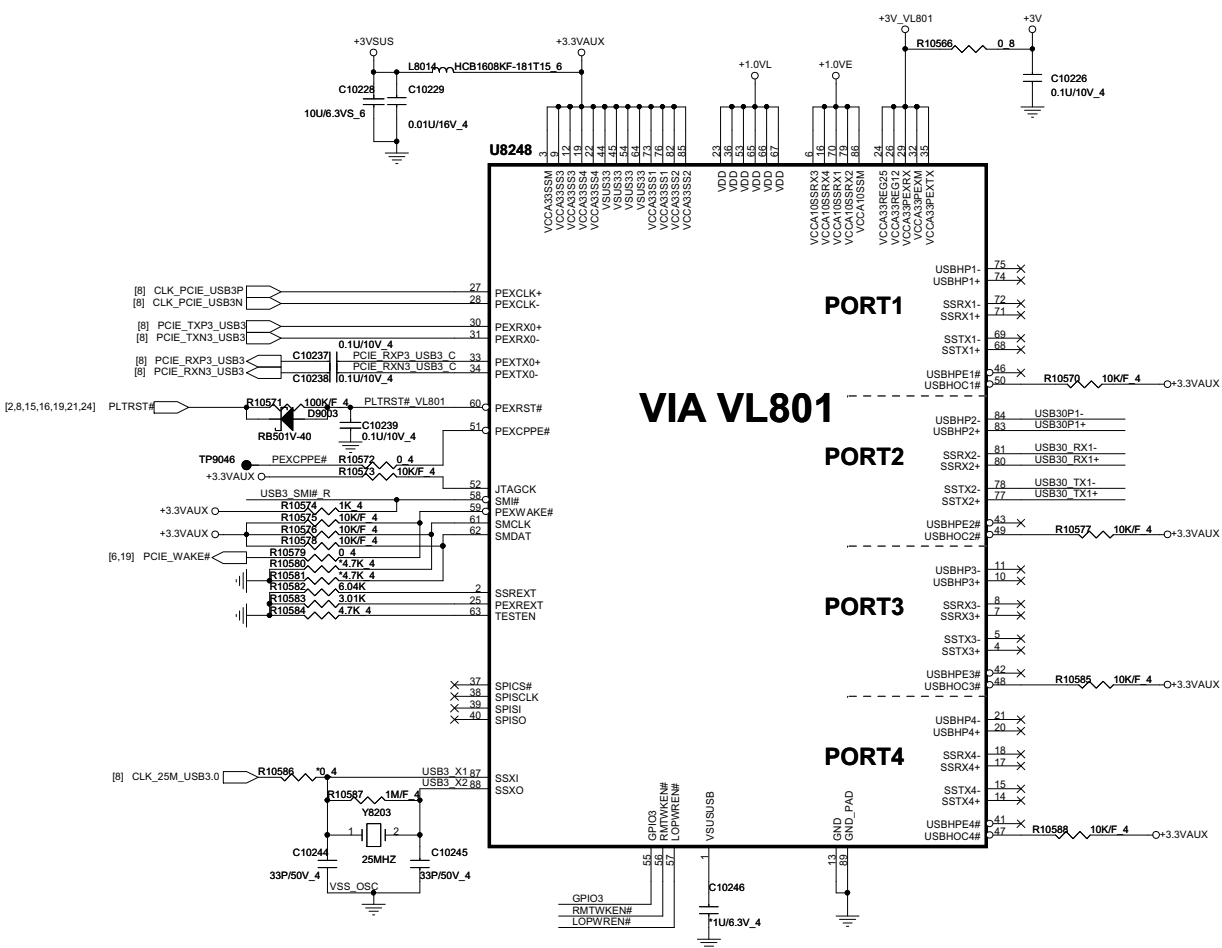
Close TO IC PIN46

**INT. SPEAKER**

|                                                                                       |  |                                                            |                  |
|---------------------------------------------------------------------------------------|--|------------------------------------------------------------|------------------|
|  |  | <b>PROJECT : LGx UMA</b><br><b>Quanta Computer Inc.</b>    |                  |
|                                                                                       |  | Size Custom<br>Document Number<br><b>HDA Azalia ALC269</b> | Rev<br><b>1A</b> |
| Date: Monday, December 05, 2011                                                       |  | Sheet 17 of 35                                             |                  |







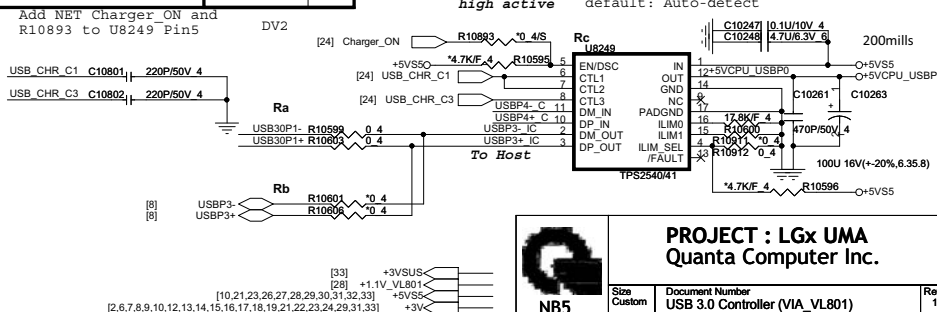
| CTL1 | CTL2 | CTL3 | TPS2540 Control Truth Table               |
|------|------|------|-------------------------------------------|
| 0    | 0    | 0    | Out Discharge ,Power switch OFF           |
| 0    | X    | 1    | Dedicated charging port, auto-detect      |
| X    | 1    | 0    | SDP1 Standard downstream port, USB 2.0    |
| 1    | 1    | 1    | Mode,SDP1 Charging downstream port, BC1.2 |

| [trans] CDP                                |         |         |         |         |
|--------------------------------------------|---------|---------|---------|---------|
| LGE SPEC                                   | S0/S3   |         | S4/S5   |         |
|                                            | AC Mode | DC Mode | AC Mode | DC Mode |
| change mode                                | CDP     | CDP     | DCP     | DCP     |
| user define Battery % and wake up from USB |         | SDP     |         | OFF     |

|        |        |
|--------|--------|
|        | Select |
| USB3.0 | Ra     |
| USB2.0 | Rb     |

### Charger USB

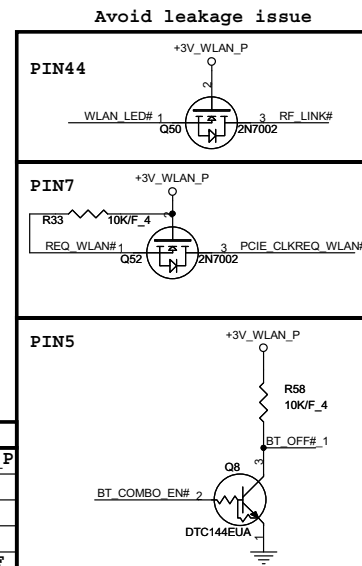
80 mils (Iout=2A)      Ios = 48000/RILIMC  
high active      default: Auto-detect



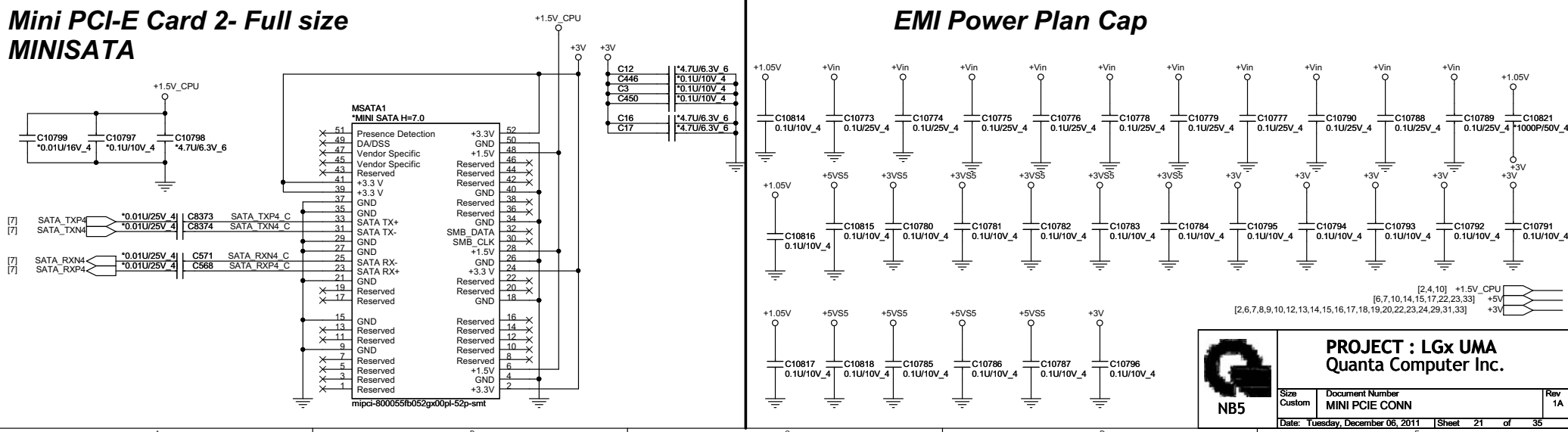
**PROJECT : LGx UMA**  
Quanta Computer Inc.

|                                  |                                                   |
|----------------------------------|---------------------------------------------------|
| Size Custom                      | Document Number<br>USB 3.0 Controller (VIA_VL801) |
| Date: Tuesday, December 06, 2011 | Sheet 20 of 35                                    |

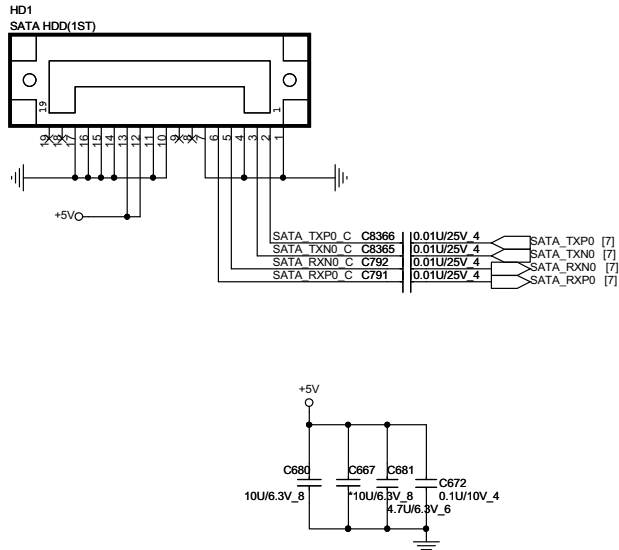
21



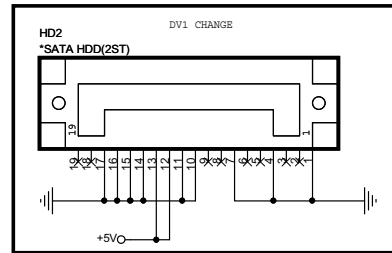
## EMI Power Plan Cap



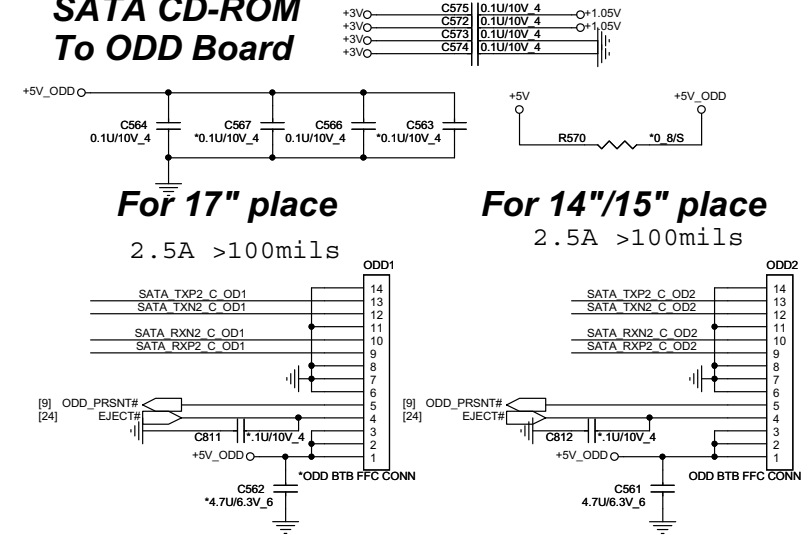
## MAIN SATA HDD



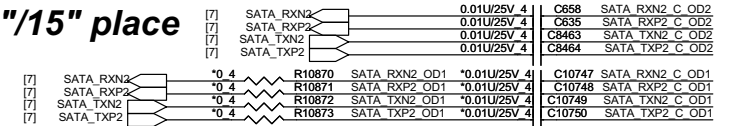
## 2nd SATA HDD for 17"



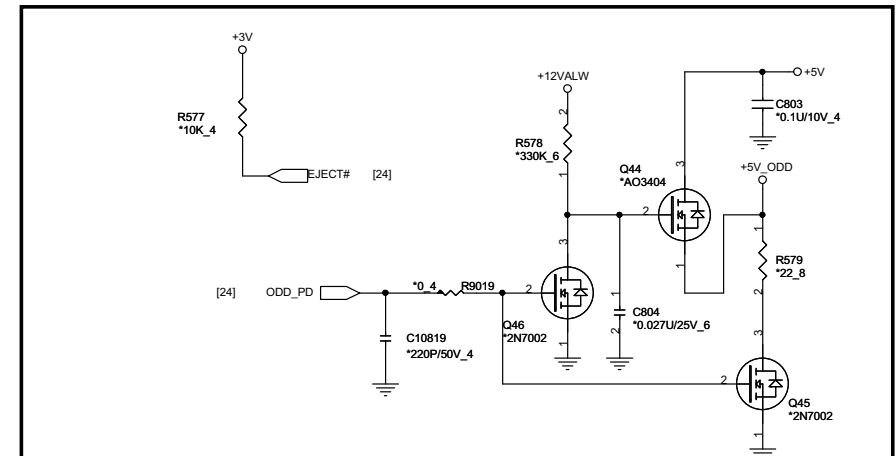
## SATA CD-ROM To ODD Board



## For 14"/15" place



## For 17" place

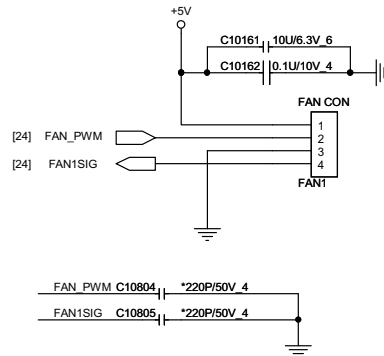


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**Quanta Computer Inc.**

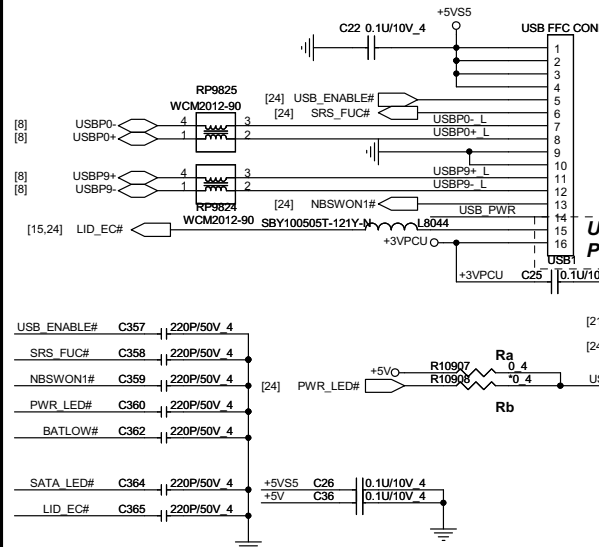
|                                                |                                  |           |
|------------------------------------------------|----------------------------------|-----------|
| Size<br>Custom                                 | Document Number<br>ODD/HDD/HOLES | Rev<br>1A |
| Date: Monday, December 05, 2011 Sheet 22 of 35 |                                  |           |

[33] +12VALW  
[6,7,10,14,15,17,21,23,33] +5V  
[2,6,7,8,9,10,12,13,14,15,16,17,18,19,20,21,23,24,29,31,33] +3V

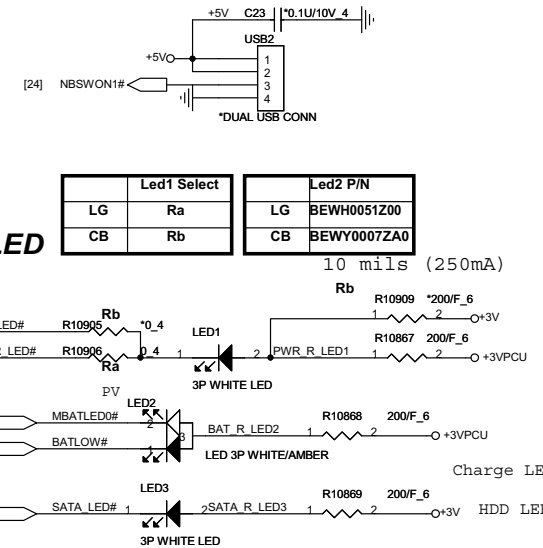
## CPU FAN



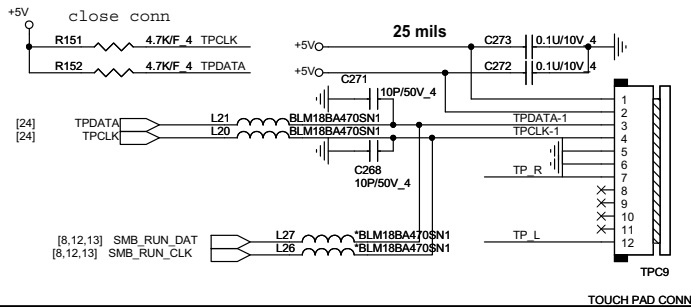
## USB / Power LED & SW for 14"/15"/17" To USB Board



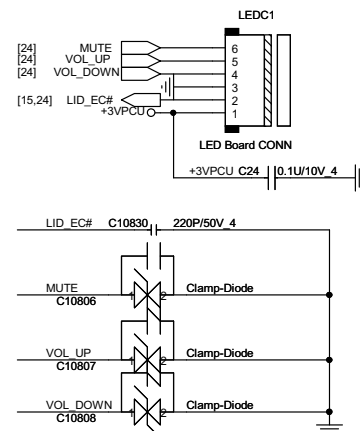
## Power SW for 17"



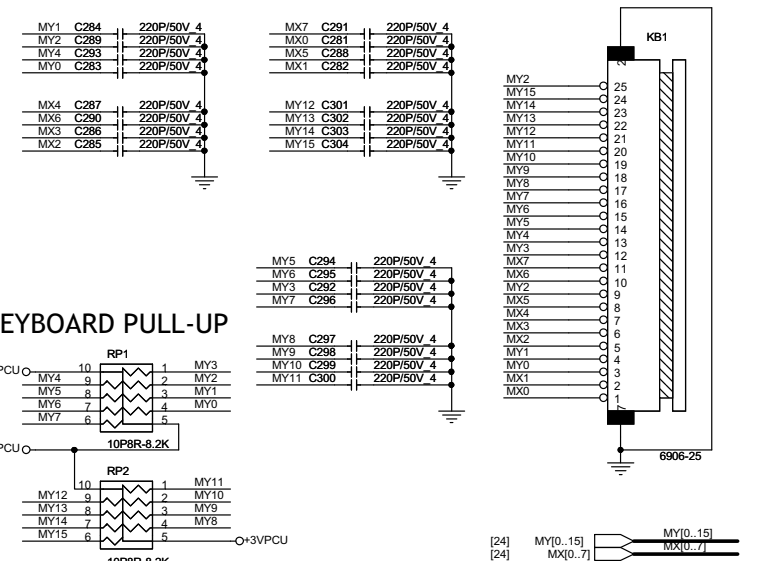
## TOUCH PAD CONNECTOR To Click Board & FP



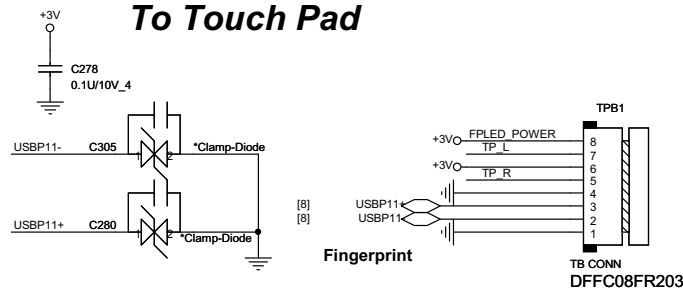
## LID / MUTE / VU UP / VU DO To AD Function Board



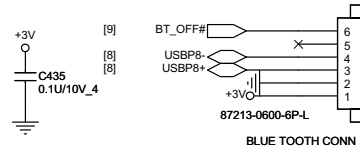
## KEYBOARD Con.



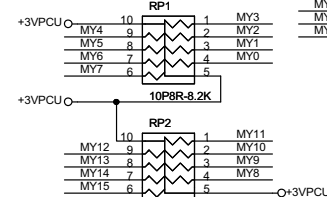
## TP Button CONNECTOR To Touch Pad



## BLUETOOTH



## KEYBOARD PULL-UP

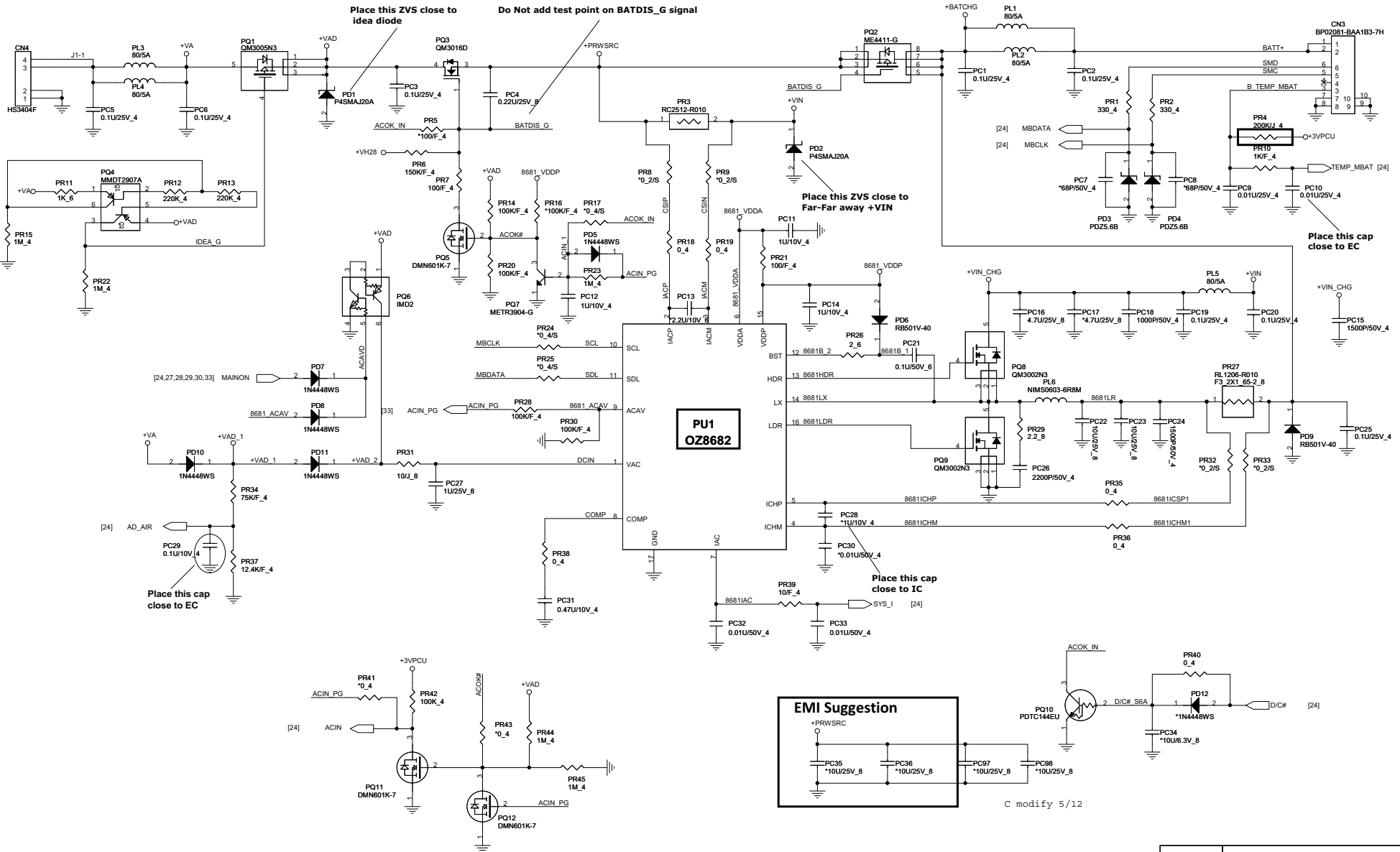


**PROJECT : LGx UMA**  
**Quanta Computer Inc.**

|                                 |                                 |           |
|---------------------------------|---------------------------------|-----------|
| Size<br>Custom                  | Document Number<br>BT/USB/eSATA | Rev<br>1A |
| Date: Monday, December 05, 2011 |                                 |           |





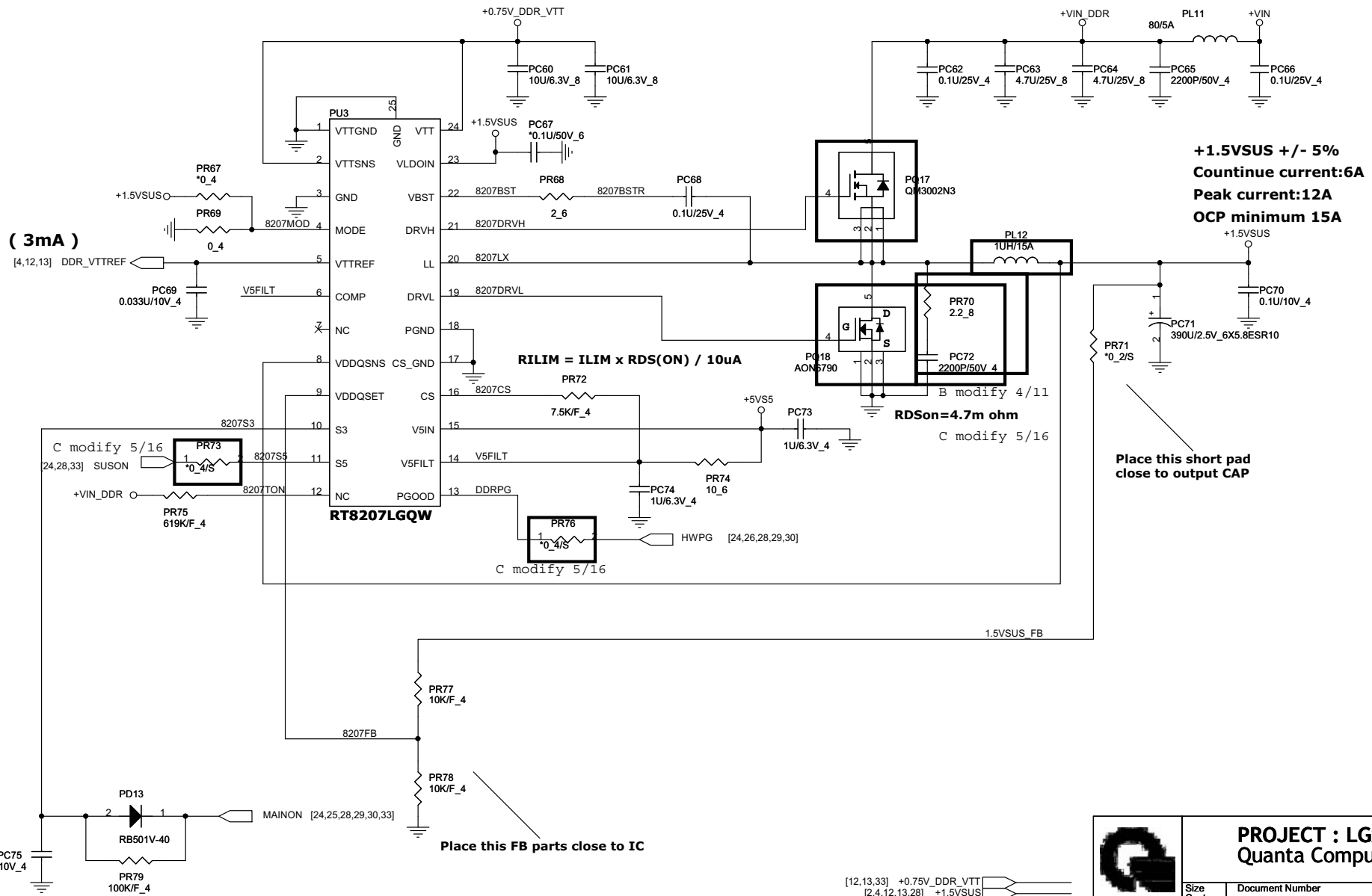
**TOP\_DC\_JACK**  
**90W/120W(QC)**

**PROJECT : LGx UMA**  
**Quanta Computer Inc.**

| Size   | Document Number         | Rev |
|--------|-------------------------|-----|
| Custon | <b>Charger (OZ8682)</b> | 1A  |

Date: Monday, December 05, 2011 Sheet 25 of 38

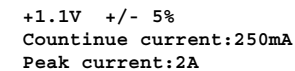
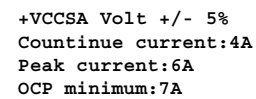


( VTT/2A )

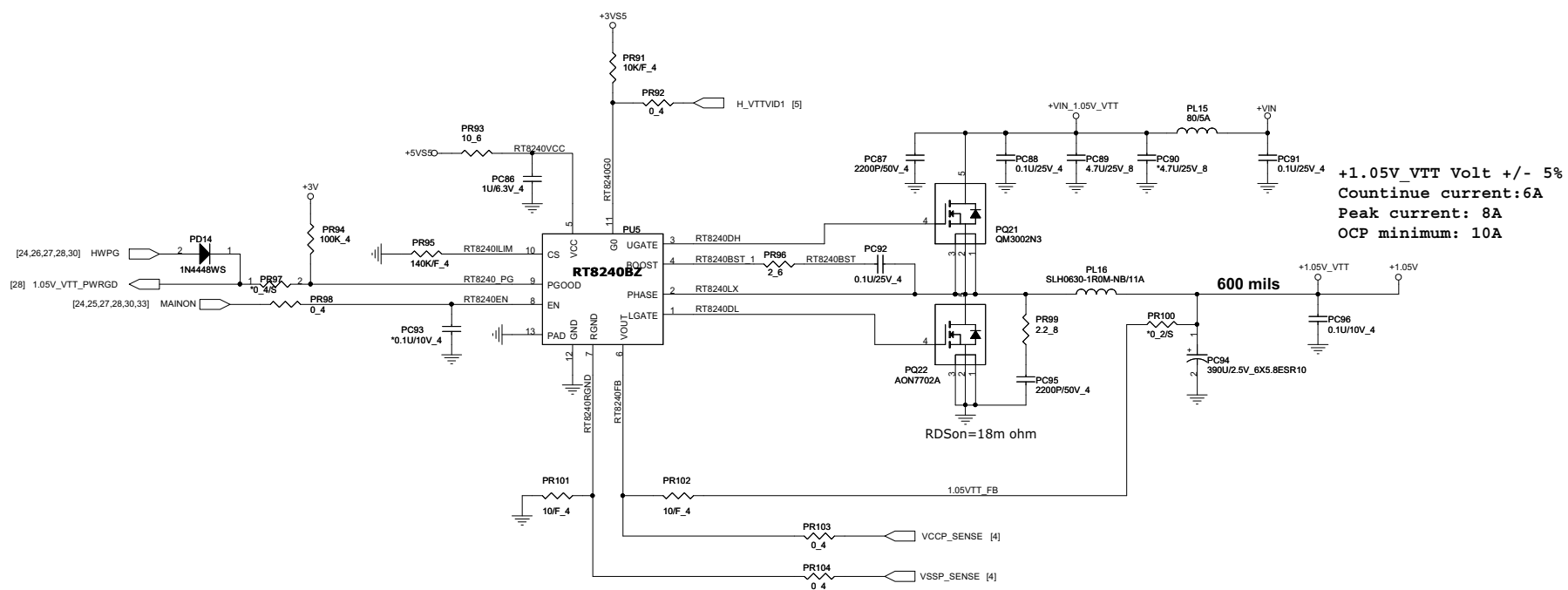


**PROJECT : LGx UMA**  
**Quanta Computer Inc.**

|                                 |                                         |           |
|---------------------------------|-----------------------------------------|-----------|
| Size<br>Custom                  | Document Number<br><b>DDR3 (RT8207)</b> | Rev<br>1A |
| Date: Monday, December 05, 2011 | Sheet 27 of 38                          |           |

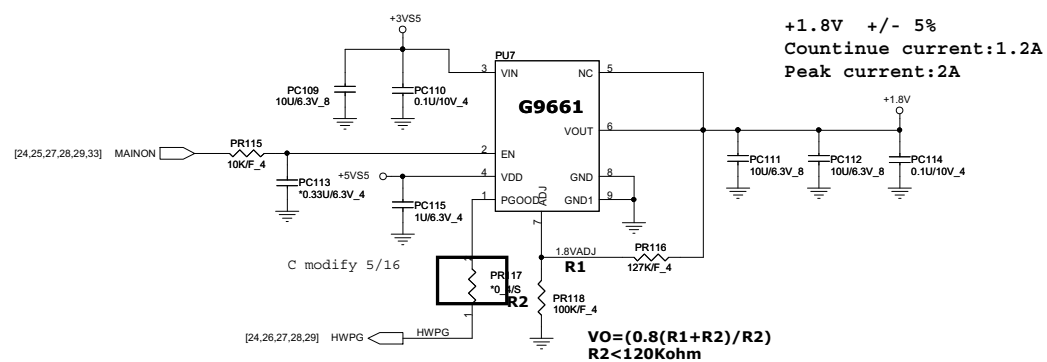


|  |  |
|--|--|
|  |  |
|--|--|



**PROJECT : LGx UMA**  
Quanta Computer Inc.

|                                 |                                               |           |
|---------------------------------|-----------------------------------------------|-----------|
| Size<br>Custom                  | Document Number<br><b>+1.05V_VTT(RT8240B)</b> | Rev<br>1A |
| Date: Monday, December 05, 2011 | Sheet 29                                      | of 38     |

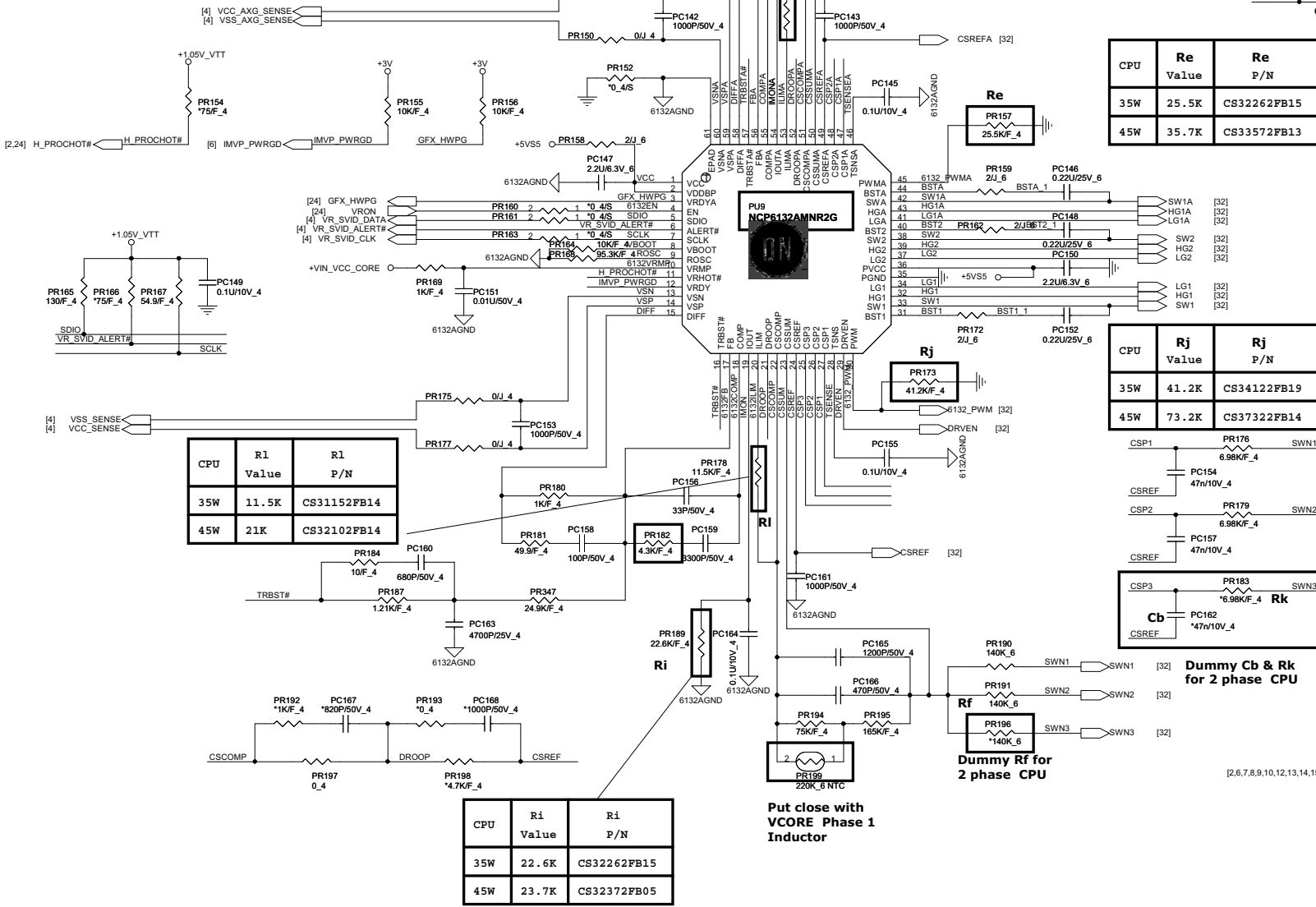


NB5

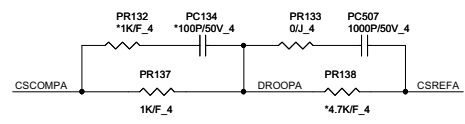
PROJECT : LGx UMA  
Quanta Computer Inc.

|                                 |                                                |           |
|---------------------------------|------------------------------------------------|-----------|
| Size<br>Custom                  | Document Number<br><b>+1.05V/+1.8V (G5173)</b> | Rev<br>1A |
| Date: Monday, December 05, 2011 | Sheet 30 of 38                                 | 1         |

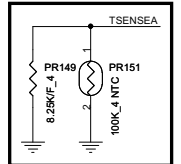
| CPU | Rg    | Rg          | Rh    | Rh          |
|-----|-------|-------------|-------|-------------|
|     | Value | P/N         | Value | P/N         |
| 35W | 21.5K | CS32152FB17 | 14K   | CS31402FB12 |
| 45W | 23.7K | CS32372FB05 | 21.5K | CS32152FB17 |



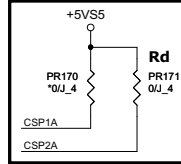
Put close with GT Inductor



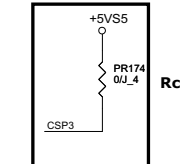
Put close with V\_GT HOT SPOT



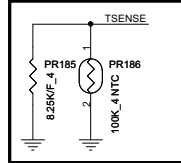
Pop Rd for GT 1-phase operation



POP Rc for 2 phase CPU



Put close with VCORE HOT SPOT



Dummy Cb & Rk for 2 phase CPU



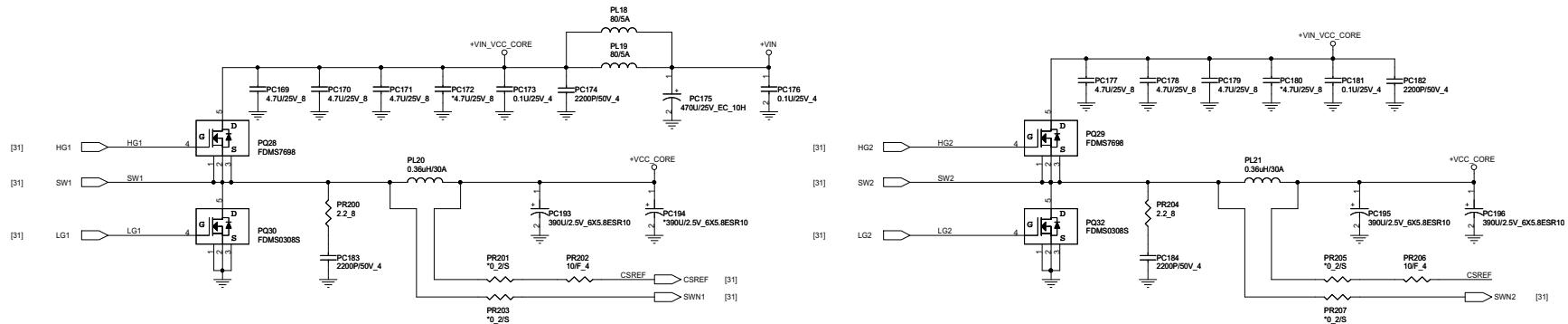
Dummy Rf for 2 phase CPU



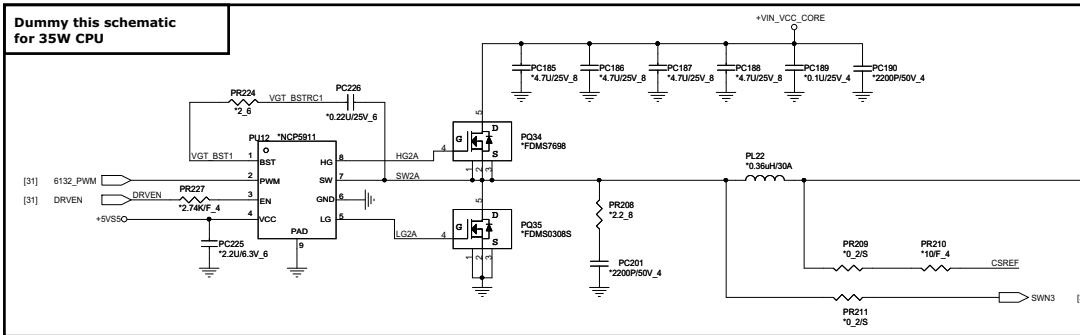
Put close with VCore Phase 1 Inductor

| CPU | Ri    | Ri          |
|-----|-------|-------------|
|     | Value | P/N         |
| 35W | 22.6K | CS32262FB15 |
| 45W | 23.7K | CS32372FB05 |

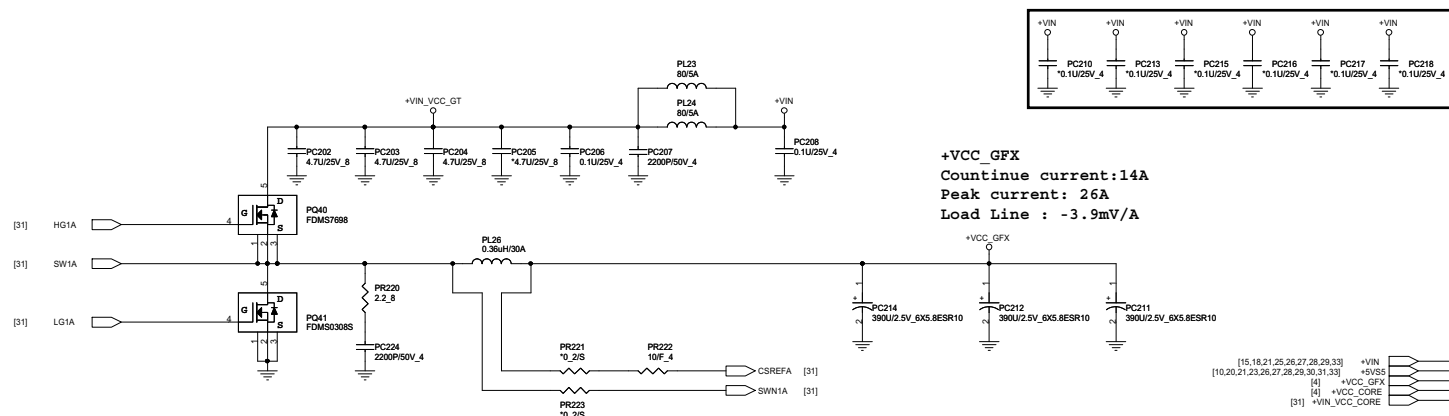
[2,6,7,8,9,10,12,13,14,15,16,17,18,19,20,21,22,23,24,29,33] +3V  
[10,20,21,23,26,27,28,29,30,32,33] +5V55  
[2,4,6,7,8,10,20,21,22,24,29] +1.05V\_VTT  
[32] +VIN\_VCC\_CORE



Dummy this schematic  
for 35W CPU



SV 35W CPU  
VID1=0.9V  
IccMax=53A  
Icc\_Dyn=43A  
Icc\_TDC=36A  
R\_LL=1.9m ohm  
OCP~60A



+VCC\_GFX  
Countinue current:14A  
Peak current: 26A  
Load Line : -3.9mV/A

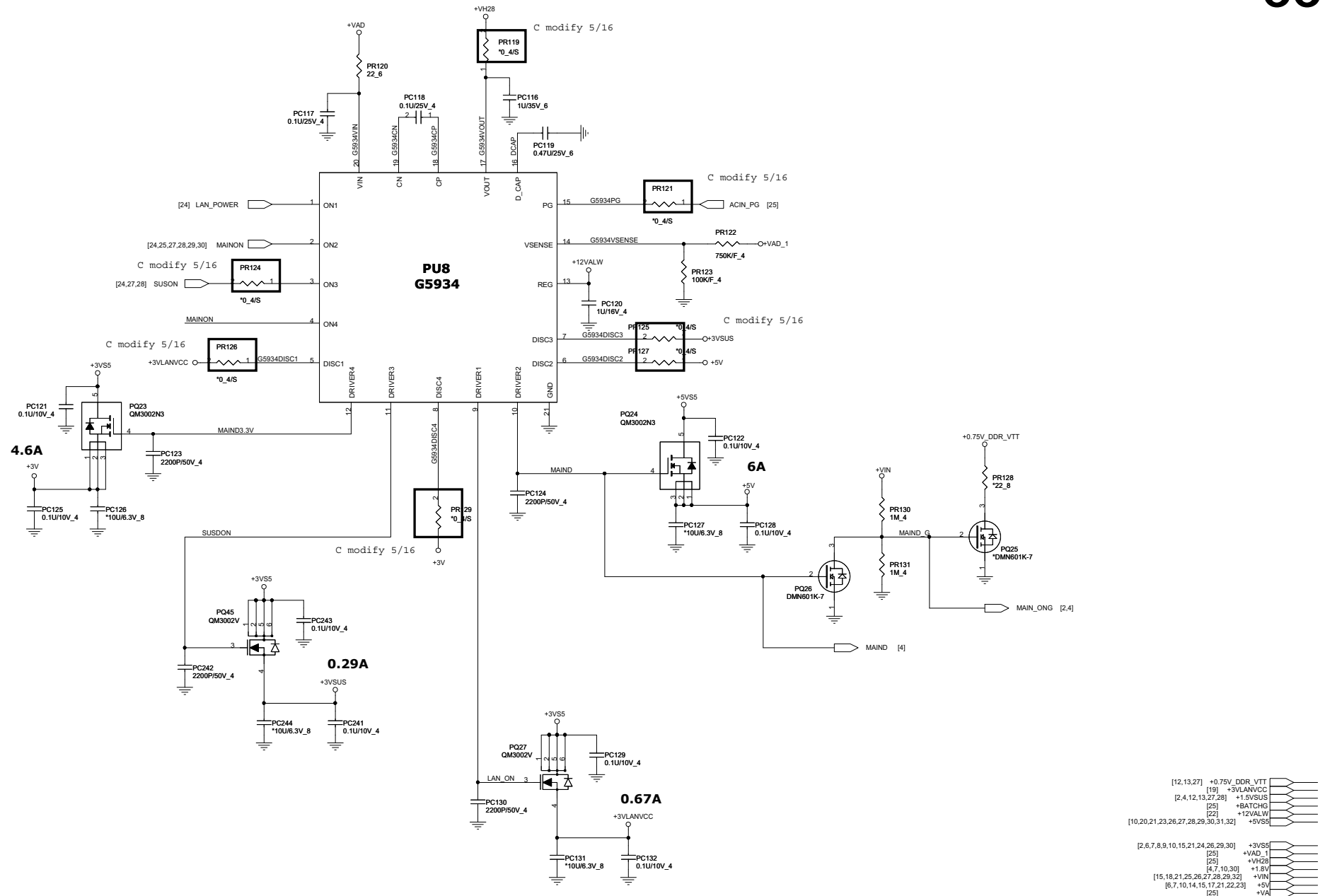
[16, 18, 21, 25, 26, 27, 28, 29, 33] +VIN  
[10, 20, 21, 23, 26, 27, 28, 29, 30, 31, 33] +VSS  
[4] +VCC\_GFX  
[4] +VCC\_CORE  
[31] +VIN\_VCC\_CORE



PROJECT : LGx UMA  
Quanta Computer Inc.

Size C Document Number CPU Core2 (NCP5911)QC Rev 1A  
Date: Monday, December 06, 2011 1 Sheet 32 of 38

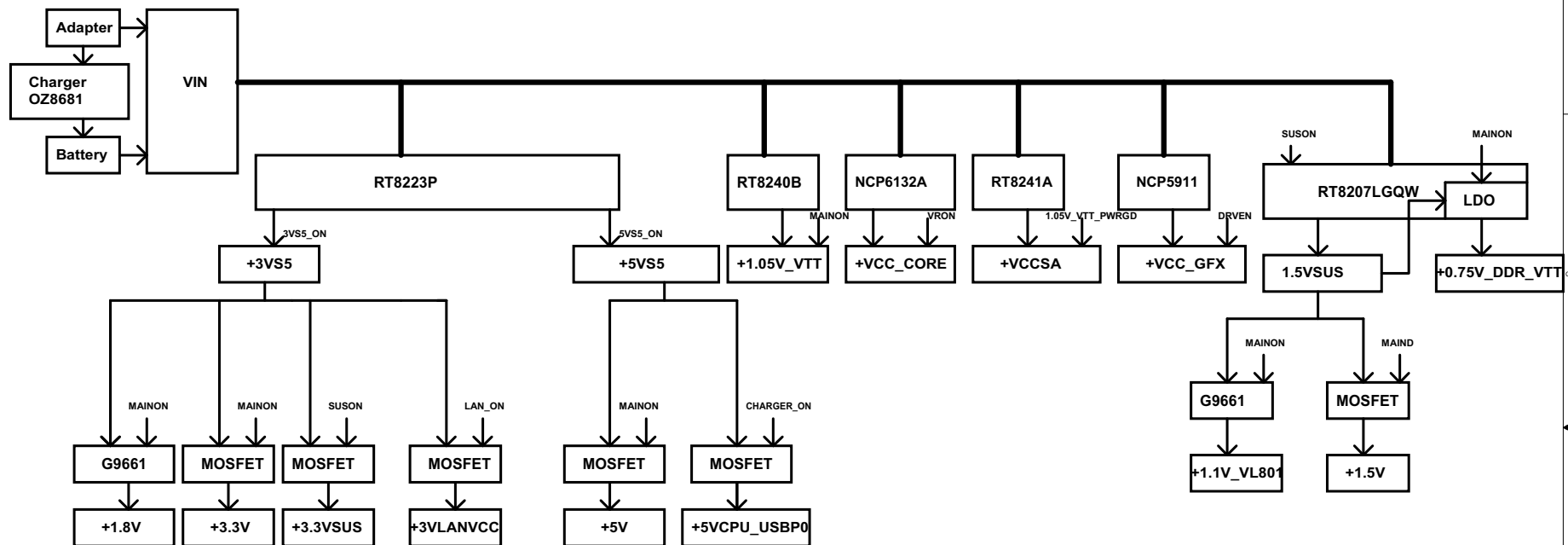




**PROJECT : LGx UMA**  
**Quanta Computer Inc.**

| Size                            | Document Number              | Rev |
|---------------------------------|------------------------------|-----|
| Custom                          | <b>Dis-charge IC (G5934)</b> | 1A  |
| Date: Monday, December 05, 2011 | Sheet 33 of 38               |     |

# LG2/4 Power rail map



NB5

PROJECT : LGx UMA  
Quanta Computer Inc.

|       |                             |                |
|-------|-----------------------------|----------------|
| Size  | Document Number             | Rev            |
|       | <b>Power Block Diagram</b>  | 1A             |
| Date: | Thursday, December 01, 2011 | Sheet 34 of 35 |

LG2/4/6 Power Sequence

